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Integration of a bidirectional cell in a quasi-Z-source inverter for CMV reduction and pure sinusoidal wave form

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Abstract

With the increasing global commitment to renewable energy sources like photovoltaics (PV), there is a critical need for high-efficiency and high-power-quality converter topologies. Traditional two-stage PV systems are often complex and introduce significant common mode voltage (CMV), leading to issues like leakage currents, high electromagnetic interference, and safety concerns. This paper proposes the integration of a bidirectional cell within a quasi-Z-source inverter (BC-qZSI) to achieve CMV reduction in a single-stage power conversion setup. The BC acts as an active balancing and filtering element rather than solely a booster, ensuring a continuous current mode and actively suppressing the high-frequency CMV components generated by the shoot-through states. The analytical mathematical expression of the proposed topology is derived to confirm its operation, voltage boost capability, and CMV characteristics. Ideal simulation results, performed using PSIM software, validate the derived expressions and demonstrate the effectiveness of the proposed design. The topology achieves a significant reduction in CMV, lowering its amplitude more than 90 % compared to the conventional qZSI. Furthermore, the output waveform quality is excellent, yielding a total harmonic distortion (THDv) of 2 %, which complies with the IEEE Std 519-2014 for acceptable waveform quality. These results confirm that the integrated BC-qZSI topology effectively mitigates CMV while maintaining high power quality and a single-stage architecture.

Keywords: quasi-Z-source inverter; single stage converter; common mode voltage.

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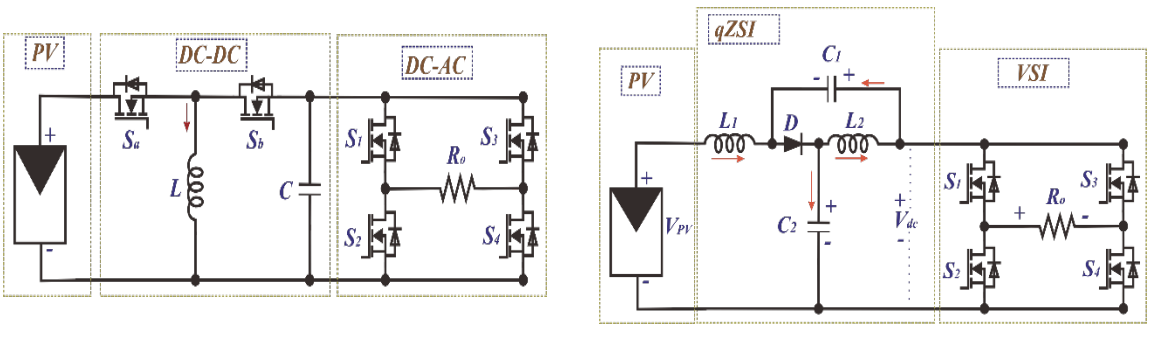
I. Introduction

The use of renewable energy sources, such as photovoltaics, wind power, and hydropower, have increased significantly in recent years due to the target of net zero emissions by 2050 [1][2][3]. Among them, the photovoltaic (PV) has been developing the fastest. Furthermore, the efficiency of commercially available PV modules, primarily those utilizing mono- and polycrystalline silicon technologies, has steadily increased to a commonly observed of 20 % to 25 % in recent years [4][5][6]. While laboratory-scale research has achieved efficiencies exceeding 45 % using advanced multi-junction and tandem cell structures, the 20 % to 25 % range is the relevant benchmark for large-scale integration into power systems. This high and continually improving efficiency makes PV technology increasingly popular among researchers and industry [7][8][9]. However, output voltage and current of the PV are fluctuating depended on the solar power source. Typically, PV panels are integrated into power systems through a two-stage power conversion setup as shown in Figure 1, comprising a DC-DC boost converter and an inverter as shown in Figure 1(a). This configuration allows for efficient energy transfer from the PV panels to the power grid. The DC-DC boost converter such as maximum power point tracking (MPPT) optimizes the voltage output from the panels, ensuring maximum power extraction under varying sunlight conditions. Subsequently, the inverter converts the DC output into AC, which is compatible with the grid. Conventional inverter topologies, such as the voltage source inverter (VSI) and current source inverter (CSI), typically require two switching devices in each inverter cell. This two-stage conversion system plays a crucial role in facilitating the integration of solar energy into the existing power infrastructure, promoting renewable energy utilization and grid stability [10][11][12]. The MPPT is used to control the fluctuative power source to maximize energy extraction of the PV. The MPPT adjusts the load characteristic to keep power transfer at the highest efficiency by sampling cell output and applying the load to obtain maximum power. MPPT topologies that use DC-DC converters such as buck, boost, buck-boost and Cuk converters are widely used in industry because the control and technology are more suitable for industry purposes. The disadvantage of this conventional MPPT is the topology only converts the power ratings from 30 % to 40 %. To overcame this problem, the researchers developed DC-DC converter topology and new technique [13][14][15] with high boost converter.

Inverter such as VSI and CSI are used to convert the MPPT output from DC to AC. Apart from PV, inverters are also used in several equipment such as AC motor drive, distribution power systems, electric vehicle and uninterruptible power supplies (UPS) [16][17]. The shortcoming of the traditional VSI is that it is operated in buck mode. The voltage at the output terminal fluctuates depending on which combination of switching devices in the inverter is turned ON. This output voltage is essentially non-sinusoidal and exhibits high total harmonic distortion (THD). When averaged over a switching period, the output voltage is consistently lower than the input voltage by an amount proportional to the duty ratio of the switches, resulting in a buck-mode operation. Therefore, the VSI requires the size and transformer to adjust with the power system specification. The frequency of power system also requires bigger transformer and higher cost. In addition, the non-sinusoidal inverter can be covered by applying filter such as LC filter. However, a two-stage power conversion setup, consisting of a DC-DC boost converter and an inverter, requires very complex control and will reduce the efficiency due to the two-stage conversion.

Several solutions were proposed to resolve the problems by using several topologies [18][19]. The inverter presented in [18], known as the Z-source



(a) (b)

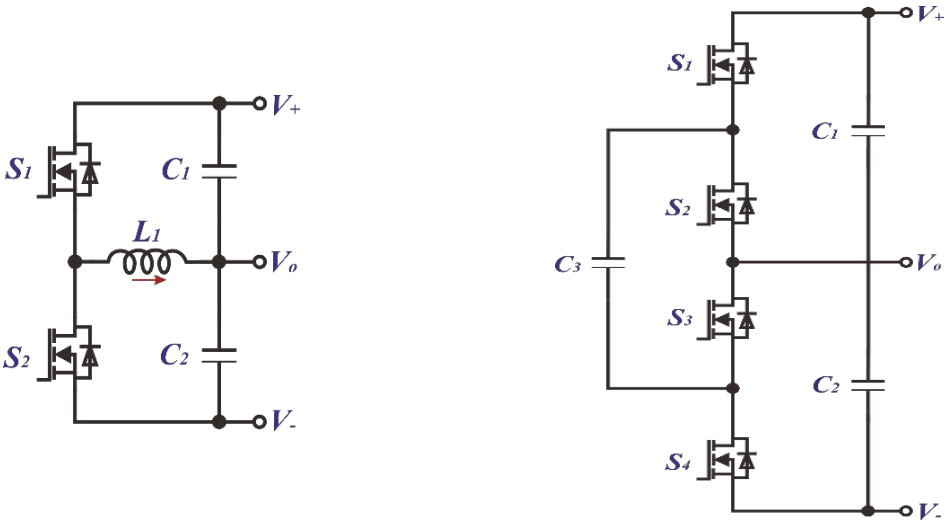
Figure 1. Single-stage and two-stage of inverter. (a) two-stage power conversion setup; (b) quasi-Z source inverter (qZSI).

inverter (ZSI), has been developed as a practical solution to overcome the common issues encountered in renewable energy systems. This converter consists of two impedances, two capacitors with X-shape components, and a traditional VSI. This converter has many advantages such as enabling short circuit or short through operation on each lag of inverter with boosting capability of inverter, single stage power conversion, and unneeded additional controls as two-stage power conversion. Nevertheless, there are some disadvantages of ZSI topology such as discontinued input current due to series connection of diode in the input ZSI that can impact the PV lifetime, high voltage stress in the capacitor, and high current ripple across inductor that can impact inductor and capacitor lifetime.

To improve the limitation of ZSI, a new topology called quasi-Z-source Inverter (qZSI) has been created [19]. The circuit topology can be seen in Figure 1(b). This topology has the same component as ZSI but the position of components is modified that allows the continue input current. The current input also flows smoothly due to series configuration between inductor and input voltage (PV). Moreover, the capacitor voltage stress and the inductor current ripple in the quasi-Z-source inverter (qZSI) are lower than in the conventional Z-source inverter (ZSI). Additionally, the qZSI shares the same ground reference as the ZSI. Although qZSI offers excellent performance, it does not offer a higher boost voltage than ZSI. Therefore, many new topologies with higher voltage boosts are proposed using multiple boost cells such as switched inductor (SL) boost cells, enhanced boost (EB) cells and embedded switched-inductor (ESL) boost cells [20][21][22]. Nevertheless, the combination of qZSI and boost cell only enhances the boost converter and forward input current which only slightly improves the limitations of two-stage power conversion. Traditional VSI still has many limitations such as non-sinusoidal output voltage and current, high total harmonic distortion (THD) and high common mode voltage (CMV). This limitation can be corrected by adding an LC filter to the inverter output so that it can improve the THD and non-sinusoidal output of the inverter with the consequence of increasing the size of the power converter and yielding expensive costs. The CMV is also not resolved by adding an LC filter. Several solutions were proposed to resolve the problems by using DC-DC converters [23][24][25]. Reference [23] proposes a new topology called the active boost inverter (ABI), also referred to as an active buck–boost inverter. This topology is suitable for wide-range input voltages and can achieve step-up (boost) conversion within a quasi-single-stage inverter configuration. The AC/AC unit includes active switches used to perform voltage boost without introducing additional passive elements, which is beneficial to the power density and efficiency of the system. Moreover, ABI also can be integrated to the qZSI condition (shoot-through condition). However, this topology needs eight switches that more complex for the control system and needs filter capacitor in the output inverter. S. Naderi and H. Rastegar [24] propose new family of highly efficient grid-tied DC/AC inverters with a wide variety of input DC voltages. This topology minimizes the voltage drop across the filter inductor in the power loop, reduces line power losses in both "boost" and "buck" modes. This topology also can be integrated in the qZSI condition but still need output and common mode filter.

Liang *et al.* [25] propose an inverter with Cuk inverter as basic cell. The advantage of this topology is the ability to reduce energy storage elements such as inductors and capacitors, thereby improving reliability and reducing size. The inherently sinusoidal Cuk inverter provides a sinusoidal output suitable for grid-connected applications. However, the configuration of Cuk inverter cannot be integrated in the qZSI condition. Parallel-Connected Partial-Power Converters (P-PPC) in [26][27] using bidirectional buck–boost converter and switched-capacitor converter as cell of DC-DC converter is shown in Figure 2. The output of those topologies is also sinusoidal with simple control. However, depending on the component, under the shoot-through state of the ZSI, C1 and C2 are momentarily shorted, which leads to a significant rise in the P-PPC current.

One approach to mitigate the drawbacks of the P-PPC converter is to remove or modify one of its two capacitors, such as C1. This configuration can be implemented in the ZSI because the capacitor (C2) is not shorted. By modifying the P-PPC converter, the P-PPC topology returns to the form of a bidirectional buck converter that is used as an active power filter due to common mode filter. Figure 3 shows the configuration of qZSI that uses APF or bidirectional buck converter as the active filter common mode of inverter. Due to the configuration of APF, the converter acting as APF is a bidirectional buck converter (BBC) that has two switches, one inductor, and one capacitor. To achieve a sinusoidal inverter output, this topology can be implemented in a quasi-Z-source inverter (qZSI). The THD, common mode ripple of inverter, also can be solved. Because of that, this configuration is suitable for qZSI.



(a) (b)

Figure 2. Parallel connected partial-power converter (P-PPC). (a) bidirectional buck–boost converter; (b) switched capacitor converter.

In this study, a PV power system based on a single-phase quasi-Z-source inverter (qZSI) integrated with a bidirectional converter is investigated. The circuit of combination of APF and qZSI can be shown in Figure 4. This combination overcomes the limitation of qZSI such as non-sinusoidal output, high common mode ripple and limitation of previous topology such as output voltage that is lower than input voltage and requiring additional DC-DC converter. BC-qZSI produces pure sinusoidal output, low CMV, higher output voltage compared to input voltage, and single stage conversion. The methodology and results will be discussed in the next section in detail.

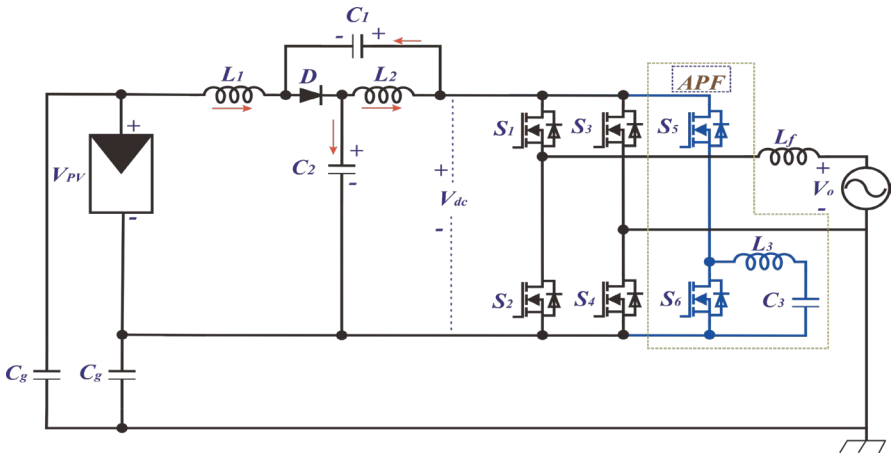


Figure 3. Active power filter (APF) qZSI.

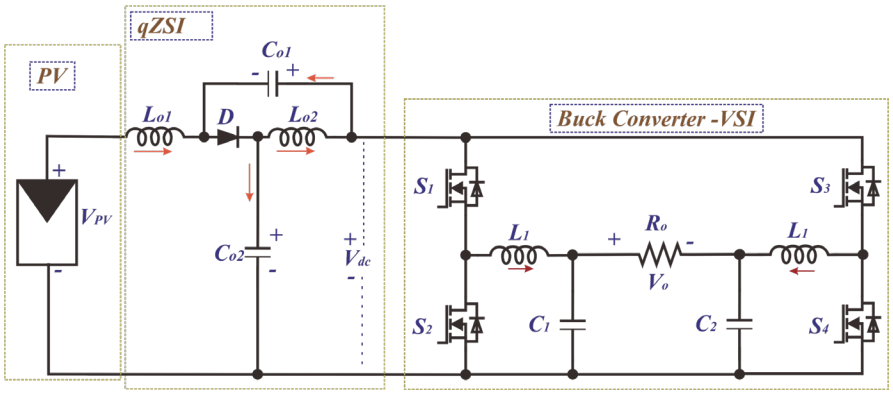


Figure 4. Bidirectional buck converter as cell of qZSI (BC-qZSI).

II. Materials and Methods

This section begins with the description of BC-qZSI. Step-by-step operation of BC-qZSI is explained and the associated mathematical analysis is expressed. The operation principle of BC-qZSI is depends on three conditions: shoot-through condition (ST), non-shoot-through condition (NST) with S1 and S4 on, and NST with S2 and S3 on. To make it easier, qZSI and bidirectional buck–boost converter is separated so that they are divided into 4 conditions where qZSI and bidirectional buck–boost converter have two conditions each. Step-by-step operatio of qZSI and bidirectional buck–boost converter is also explained and the associated mathematical analysis is expressed.

A. Circuit analysis of qZSI

The qZSI converter in Figure 4 consist of two inductors (Lo1 and Lo2), two capacitors (Co1 and Co2), and one diode (D). The following analysis considers the characteristics of the steady-state converter, the ideal component characteristics, and the capacitance and inductance of the capacitor and inductor which are assumed to be the same. As explained above, qZSI has two conditions namely ST conditions and NST conditions as shown in Figure 5. In the ST state all of switches in the inverter are short circuited and in the NST state one of switches in the inverter are open.

In the ST state ($0 < t < t_{ST}$) the diode is open, all of switches are on, voltage of inductor (Lo1) and V_{Co1} are in a series condition and parallel with the voltage inductor (Lo2) and V_{Co2} as shown in Figure 5(a). The output voltage (V_{DC}) is zero due to the short circuit of the quasi-Z-source inverter. The corresponding inductor and output voltage to this state can be written as equation (1):

$$\begin{cases} V_{L_{o1\_ST}} = V_{PN} + V_{Co1} \\ V_{L_{o2\_ST}} = V_{Co2} \\ V_{dc\_ST} = 0 \end{cases} \quad (1)$$

In NST state ($t_{ST} < t < T$), the diode is open, the VPV and voltage of inductor (Lo1) are in a series condition and parallel with the V_{Co2}. The voltage inductor (Lo2) and V_{Co2} are parallel with V_{DC}, and voltage inductor (Lo2) is parallel with V_{Co1} as shown in Figure 5(b). The corresponding inductor and output voltage to this state can be written as equation (2):

$$\begin{cases} V_{L_{o1\_NST}} = V_{PN} - V_{Co2} \\ V_{L_{o2\_NST}} = V_{Co1} \\ V_{dc\_NST} = V_{Co1} + V_{Co2} \end{cases} \quad (2)$$

By using second voltage balance principle, the average voltage of inductor in the steady state is zero. From equation (1) and equation (2) the average voltage inductor can be described as in equation (3) and from equation (3) the average voltage of capacitor (V_{Co1} and V_{Co2}) can be described as in equation (4).

$$\begin{cases} \overline{V_{L_{o1}}} = \frac{1}{T}\left(\int_0^{t_{ST}} V_{L_{o1\_ST}} dt + \int_{t_{ST}}^{T} V_{L_{o1\_NST}} dt\right) = 0 \\ \overline{V_{L_{o2}}} = \frac{1}{T}\left(\int_0^{t_{ST}} V_{L_{o2\_ST}} dt + \int_{t_{ST}}^{T} V_{L_{o2\_NST}} dt\right) = 0 \end{cases} \quad (3)$$

$$\begin{cases} V_{Co1} = \frac{D}{1-2D} V_{PV} \\ V_{Co2} = \frac{1-D}{1-2D} V_{PV} \end{cases} \quad (4)$$

From equation (2) to equation (4) the DC value (V_{PV}) on the output voltage (V_{DC}) can be written as equation (5):

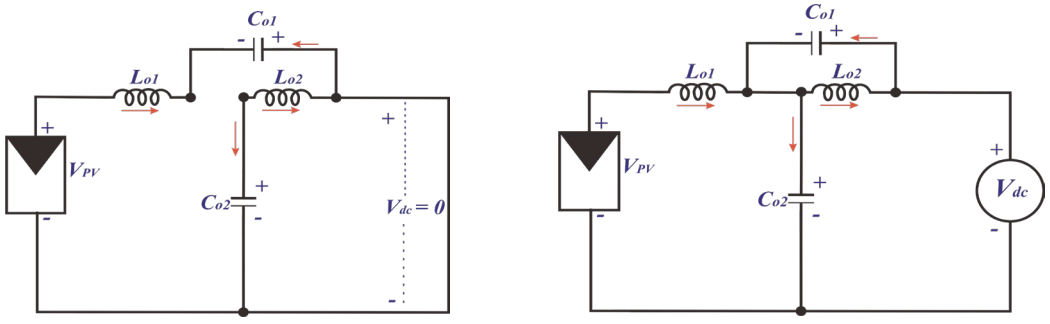
$$V_{DC} = \frac{1}{1-2D} V_{PV} \quad (5)$$

where D is shoot-trough duty ratio of qZSI, V_{PV} is DC input voltage on the PV. The boost factor (B) in the qZSI can be written as equation (6):

$$B = \frac{V_{DC}}{V_{PV}} = \frac{1}{1-2D} \quad (6)$$

B. Bidirectional converter analysis

The bidirectional converter as cell of single-phase full bridge inverter is operated in the NST condition. The following analysis considers the characteristics of the steady-state converter, the ideal component



(a) (b)

Figure 5. Operation principle of quasi-Z-Source Inverter. (a) shoot-through (ST) state; (b) non-shoot-through (NST) state.

characteristics, and the capacitance and inductance of the capacitor and inductor which are assumed to be the same. The bidirectional converter also has two state conditions which are state 1 and state 2 shown in Figure 6.

In the state 1 condition, the switches S1 and S4 are in on condition and switches S2 and S3 in off condition. The passive component C1 and L1 are parallel to V_{DC}. L2 and C2 are parallel. The inverter output is the voltage difference between C1 and C2. The mathematical expression of Kirchhoff's voltage law (KVL) in the state 1 condition can be written as equation (7) and equation (8):

$$\begin{cases} L1\_1 = V_{DC} - V_{C1} \\ V_{L2\_1} = -V_{C2} \end{cases} \quad (7)$$

$$V_o = V_{C1} - V_{C2} \quad (8)$$

In the state 2 condition, the switches S2 and S3 are in on condition and switches S1 and S4 in off condition. The passive component C1 and L1 are parallel. L2 and C2 are parallel to V_{DC}. The output inverter is voltage difference between C1 and C2. The mathematical expression of Kirchhoff's Voltage Law (KVL) in the state 2 condition can be written as equation (9) and equation (10):

$$\begin{cases} V_{L1\_2} = -V_{C1} \\ V_{L2\_2} = V_{DC} - V_{C2} \end{cases} \quad (9)$$

$$V_o = V_{C1} - V_{C2} \quad (10)$$

By using the same principle as qZSI, second voltage balance principle, the average voltage of inductor in the steady state is zero. Therefore, from equation (7) to equation (9) the average of inductor voltage can be described as equation (11):

$$\begin{cases} V_{C1} = dV_{DC} \\ V_{C2} = (1-d)V_{DC} \end{cases} \quad (11)$$

As shown in equation (8) to equation (10), the output voltage of inverter is voltage difference between V_{C1} and V_{C2}. Thus, the output voltage of the inverter can be described as equation (12):

$$\begin{aligned} V_o &= V_{C1} - V_{C2} \\ V_o &= (2d-1)V_{DC} \end{aligned} \quad (12)$$

where d is duty ratio of the inverter. The value of duty ratio inverter (d) is different from ST duty ratio of qZSI (D).

C. Inverter analysis

In the sinusoidal pulse width modulation (SPWM) strategy the modulation signal of inverter uses sinusoidal wave form as the reference signal. The modulating signal (m) is changed from 1 to -1. But the signal received by the switch is the duty ratio (d) that can be assumed by any value between 1 and 0. Thus, the difference between signal modulation and duty ratio needs to be obtained by a relationship equation. The relationship between the magnitude of the modulating signal and the duty ratio can be described as equation (13) and equation (14):

$$m = 2d - 1 \quad (13)$$

$$d = \frac{1+m}{2} \quad (14)$$

Substituting equation (14) to the equation (11) and equation (12) the capacitor voltage can be described as equation (15):

$$\begin{cases} V_{C1} = \left(\frac{1+m}{2}\right) V_{DC} \\ V_{C2} = \left(\frac{1-m}{2}\right) V_{DC} \end{cases} \quad (15)$$

From equation (15), the output voltage of inverter can be written as equation (16):

$$\begin{aligned} V_o &= V_{C1} - V_{C2} \\ V_o &= mV_{DC} \end{aligned} \quad (16)$$

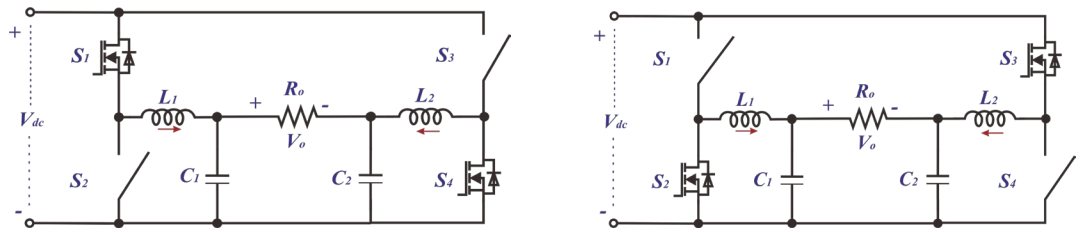
with equation (17)

$$m = v_m \sin \omega t \quad (17)$$

where v_m is amplitude of modulation signal ($v_m \leq 1$).

D. Modulation method

The modulation method used for the BC-qZSI is a straightforward extension of the conventional SPWM used in qZSI. It incorporates the short-through (ST) state, resulting in two shoot-through conditions within each switching period, as illustrated in Figure 7. The ST duty ratio of qZSI is limited by modulation



(a) (b)

Figure 6. Operation principle of bidirectional converter. (a) state 1 (S1 and S4 ON); (b) state 2 (S2 and S3 ON).

signal. The mathematical equation for the ST duty ratio between the magnitude of the modulating signal can be written as equation (18):

$$D \leq 1 - m \tag{18}$$

The peak of output voltage inverter is described in equation (19) and from that equation the voltage gain is written in equation (20).

$$V_{o\_peak} = mV_{DC} = mBV_{PV} \tag{19}$$

$$G = \frac{V_o}{V_{PV}} = mB \tag{20}$$

III. Results and Discussions

In this section, the results as voltage output, combination as qZSI and bidirectional converter, CMV, boost factor, comparative analysis, and simulation result will be discussed in detail. The graphic for boost factor and voltage gain also will be analyzed with best factor of boost as illustrated in Figure 8. The analysis also includes the common-mode ripple and the THD of the BC-qZSI output voltage, evaluated using FFT to observe the inverter's fundamental frequency component. The power rating and efficiency will be discussed in the next stage of experimental results and non-ideal system of BC-qZSI.

A. Boost factor analysis

Substituting the modulation index in equation (18) to the boost factor in equation (6), the boost factor of this topology to the index modulation can be written as equation (21):

$$B = \frac{1}{2m-1} \tag{21}$$

Figure 8(a) shows the boost factor using modulation index. The boost factor value becomes 25 times at a modulation index of 0.52. The output of boost factor is in the range of $0.5 \leq m \leq 1$ and the maximum of boost of qZSI is equal to 0.5.

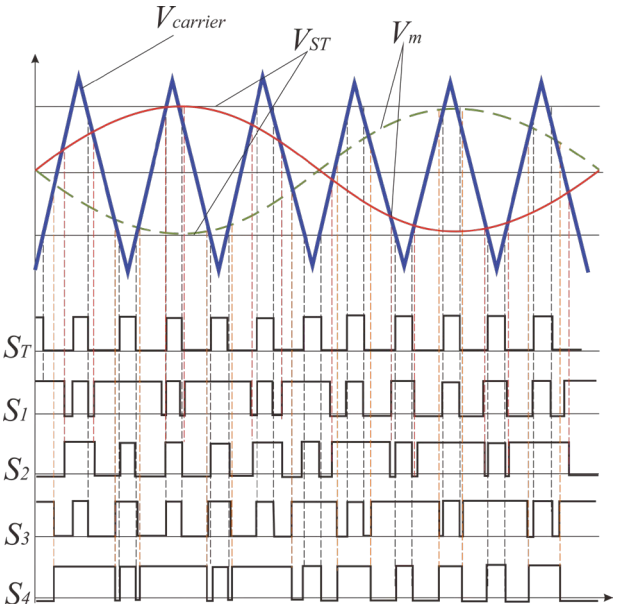
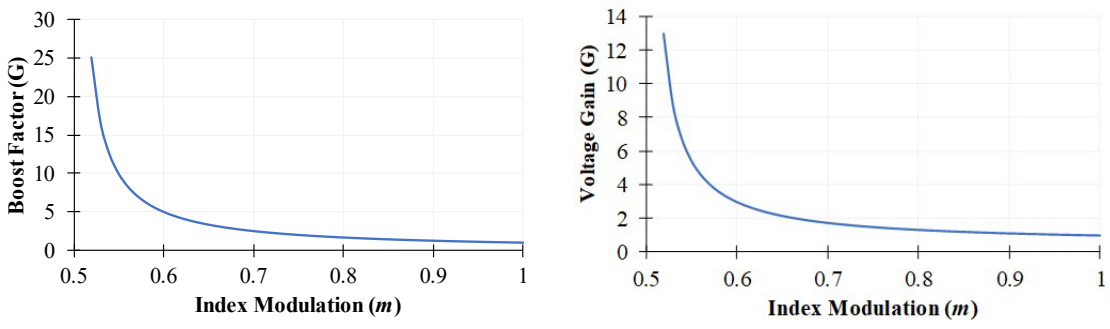


Figure 7. Modulation method.



(a) (b)

Figure 8. (a) boost factor; and (b) voltage gain of BC-qZSI.

B. Voltage gain analysis

Substituting the voltage gain in equation (20) to the boost factor in equation (21), the voltage gain of this topology to the index modulation can be written as equation (22):

$$G = \frac{m}{2m-1} \tag{22}$$

Same as boost factor, Figure 8(b) shows the voltage gain using modulation index. The value of voltage gain of BC-qZSI becomes 13 times at a modulation index of 0.52. The output of boost factor is in the range of $0.5 \leq m \leq 1$ and maximum of boost of qZSI occurs at the modulation index value of 0.5.

C. Common mode ripple voltage analysis

Generally, CMV problem occurs when the converter is isolated with the galvanic material. The different voltage of neutral load and ground of power source is called as CMV or capacitor voltage in ground system (v_{C_g}). The CMV of conventional single-phase inverter can been seen in Figure 1(b). During switching in a single-phase inverter, the common-mode voltage corresponds to the neutral point of the qZSI output voltage. If the inverter operates with a high switching frequency, the CMV also has a high frequency. If the CMV is high, the capacitive leakage current returns to the source due to the interaction between the high rate of change of the CMV, and the inherent leakage capacitance will also be high. This can lead to undesirable situations, such as nuisance ground current protection. This condition makes the unwanted current from ground to the neutral. From Figure 1(b), the CMV of qZSI can be written in equation (23). Equation (23) shows that the CMV of single-phase inverter occurs at the voltage of switch as well as S2 or S4. The current of common mode also can be written in equation (24).

$$v_{cm} = \frac{v_{ag}+v_{bg}}{2} = \frac{V_{DC}}{2} = v_{C_g} \tag{23}$$

$$i_{cm} = \frac{dv_{C_g}}{dt} C_g \tag{24}$$

where v_{ag} is the voltage between positive output and ground while v_{bg} is the voltage between ground. ω_{cm} is the value with frequency switching of the inverter. In the proposed qZSI inverter, the CMV is the sum of the voltage on capacitor v_{C1} and the voltage on capacitor v_{C2}, divided by two as shown in equation (25). Similar to the current of common mode conventional qZSI, the current of common mode is written in equation (24).

$$v_{cm} = \frac{v_{ag}+v_{bg}}{2} = \frac{v_{C1}+v_{C2}}{2} = \frac{V_{DC}}{2} = v_{C_g} \tag{25}$$

D. Simulation result

To provide the mathematical analysis of the proposed inverter the simulation of BC-qZSI is calculated using PSIM software. The parameters of simulation BC-qZSI are shown in Table 1. The capacitor, inductor, diode and switch are assumed as parasitic components such as equivalent series resistance (ESR) of capacitors and inductors, forward voltage diode, diode resistance, and on-resistance of the switch to approximate real conditions. The parasitic component of diode follows MSC010SDA070K and the switch follows STB10LN80K5 as displayed in Table 1. The proposed topology operates at a frequency of 10kHz, though using higher or lower frequencies is also feasible. The choice of frequency primarily impacts the losses in the switch, diode, capacitor, and inductor. Generally, lower switching frequencies result in higher losses in the inductor and capacitor, while higher frequencies increase losses in the diode and switch. However, the losses of switching frequency of proposed topology are not discussed in this research. The output voltage is selected using the modulation index so that output voltage is 220 Vrms. From Table 1, the input voltage of BC-qZSI is 100 VPV. The modulation index used was 0.6 that has output value as 447 VDC. The output of

Table 1.
Parameters simulation of BC-qZSI.

Parameters	Value	Parameters	Value
Input voltage of qZSI (VPV)/VDC	100 Volt	Capacitors (Co1 and Co2)	470 µF
Output voltage of qZSI	500 Volt	Capacitors (C1 and C2)	10 µF
Inverter output (Vo)/VAC	300 Vp	Inductors (L1 and L2)	1 mH
Modulation index (m)	0.6	Inductors (Lo1 and Lo2)	2 mH
Switching frequency fs/kHz	10	Load resistance Rload/ Ω	50
Fundamental frequency ff/Hz	50	Power rating/W	775
ESR of capacitors/ Ω	10m	ESR of inductors/ Ω	0.51
Diode forward voltage/V	1.5	diode resistance/ Ω	400m
On-resistance of the switch/ Ω	0.65	Switch forward voltage/V	1.5

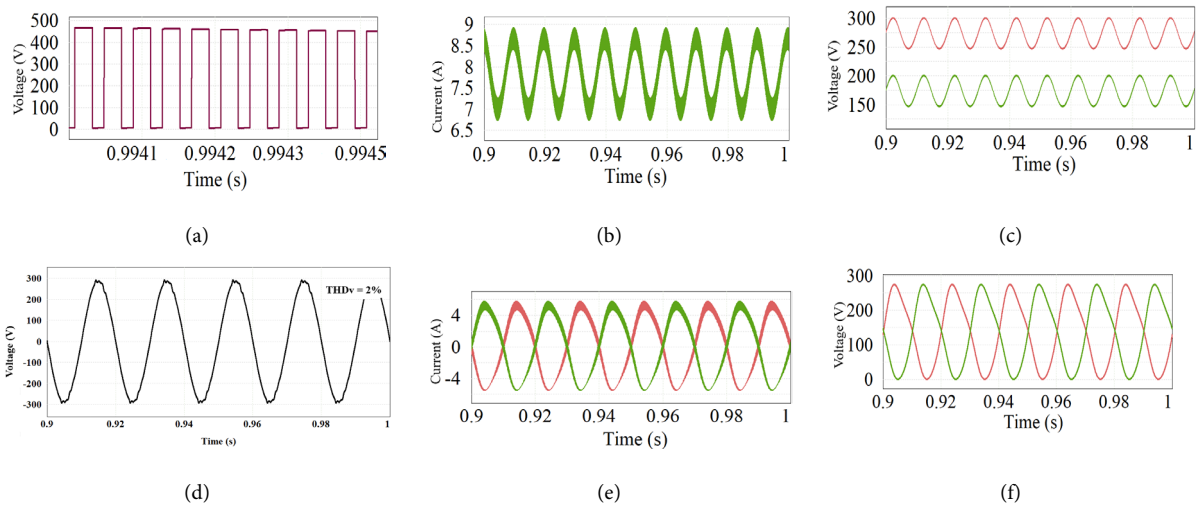


Figure 9. Simulation result of BC-qZSI. (a) output voltage of BC-qZSI (VDC); (b) inductors current (Lo1 and Lo2); (c) capacitors voltage (Co1 and Co2); (d) inverter output (Vo); (e) inductors current (L1 and L2); (f) capacitors voltage (C1and C2).

inverter is 261.7 Vp, which is approximately 185 Vrms. The voltage drop occurs due to the parasitic components of proposed topology. Figure 9 presents the simulation result such as output voltage, current inductors, and voltage capacitor of BC-qZSI. Figure 9(a)-(c) shows the output voltage, inductor current and capacitor voltage on the qZSI side. Figure 9(d)-(f) shows the output voltage, inductor current and capacitor voltage on the inverter side (BC as leg inverter).

Figure 9(a) shows the output voltage of qZSI with the modulation index of 0.6 and ST duty ratio 0.4. The output voltage of BC-qZSI is 447 V where input voltage of BC-qZSI is 100 Volt. The current of inductor (Lo1 and Lo2) in qZSI is also presented in Figure 9(b) that has same value of 7.75 A and frequency 100 Hz due to the sum of the values of L1 and L2. Figure 9(c) shows the voltage capacitor of qZSI that has capacitor voltage average as Co1 = 173.57 Volt and Co2 = 273.5 Volt. The voltage drops of capacitors occurs due the parasitic components of the topology. The inverter output, as shown in Figure 9(d) is the output voltage of 523.4 Volt peak to peak or 185 Vrms. The current inductors (L1 and L2), as shown in Figure 9(e), have the same rms current of 4 A. The voltage capacitors of BC-qZSI as shown in Figure 9(f) have the same value (C1 and C2 = 136.5Vdc) with sinusoidal voltage of 261.7 Volt peak to peak. The output voltage capacitor is pure sinusoidal, verified in equation (15). The different phase between C1 and C2 is 180°. The comparison of simulation results and mathematical analysis can be seen in Table 2. Table 2 shows that the simulation result and mathematical analysis have unequal values due to the parasitic components of topology. However, the simulation results verify the mathematical analysis of BC-qZSI. As shown in Table 1, the power rating of the proposed topology is calculated as 775 Watt.

E. Comparative analysis of BC-qZSI with conventional qZSI

A comparative analysis between the proposed BC-qZSI and the conventional qZSI [16] was conducted to evaluate the power quality. The output voltage waveforms and their corresponding FFT spectra are presented in Figure 10. Figure 10(a) illustrates the

Table 2.
Comparative analysis mathematical and simulation result of BC-qZSI.

Parameters	Value	
	Mathematical	Simulation
Input voltage of qZSI (VPV)/Vdc	100	100
Output voltage of qZSI (VDC)/Vdc	500	447
Inverter output (Vo)/VAC	300	261.7
Modulation index (m)	0.6	0.6
Shoot-trough duty ratio (D)	0.4	0.4
Voltage capacitors (Co1 and Co2)/Vdc	200 and 300	173.57 and 273.5
Voltage capacitors (C1 and C2)/Vdc	150 Vdc	136.5 Vdc

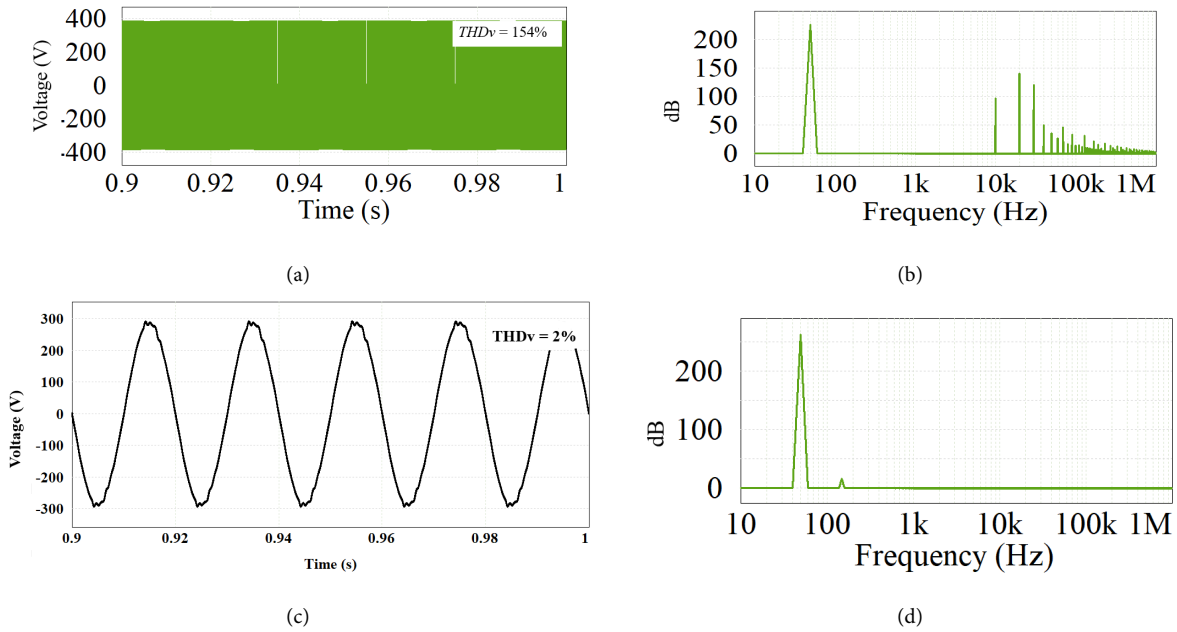


Figure 10. Output waveform and FFT of qZSI and BC-qZSI. (a) Output waveform of qZSI; (b) FFT of qZSI; (c) Output waveform of BC-qZSI; (d) FFT of BC-qZSI.

output of the conventional qZSI which exhibits a characteristic square waveform. This is corroborated by the FFT analysis in Figure 10(b) which reveals a fundamental frequency at 50 Hz accompanied by significant harmonic content at twice the switching frequency (10 kHz) and its multiples. Consequently, the conventional topology yields a high THD_v of 154%, indicating poor waveform quality. In contrast, the proposed BC-qZSI generates a high-quality sinusoidal output, as shown in Figure 10(c). The corresponding spectral analysis in Figure 10(d) demonstrates a substantial reduction in high-frequency harmonics compared to the conventional topology. Quantitatively, the BC-qZSI achieves a significantly lower THD_v of 2 %. This value is well within the limits established by IEEE Std 519-2014, which recommends a THD_v below 5 % for acceptable waveform quality at the point of common coupling. These results validate that the proposed topology offers superior harmonic performance compared to the conventional qZSI.

The CMV, common mode current between BC-qZSI and conventional qZSI also was analysed as shown in Figure 11. Figure 11(a) shows the CMV of qZSI. The ripple CMV of qZSI is equal to 400 Volt. This means that the dv/dt value at CMV is very high. By using equation (24) the common mode current ripple must be high as shown in Figure 11(b). The

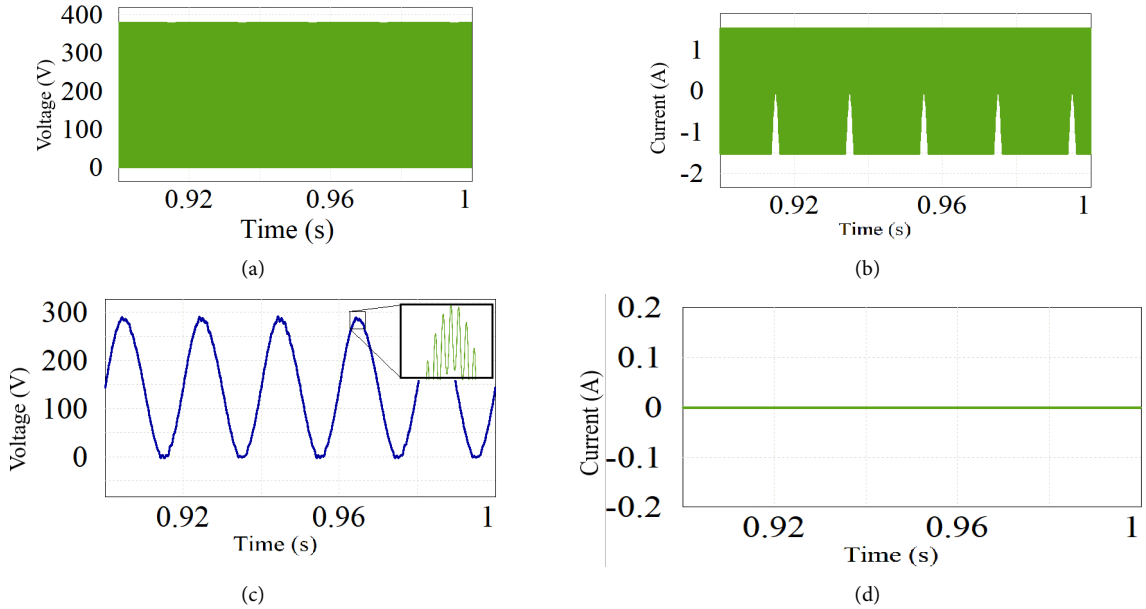


Figure 11. Common mode voltage and current of qZSI and BC-qZSI. (a) Common mode voltage of qZSI; (b) Common mode current of qZSI; (c) Common mode voltage of BC-qZSI; (d) Common mode current of BC-qZSI.

ripple current common mode is equal to 3A peak to peak. The CMV of BC-qZSI is shown in Figure 11(c). The CMV ripple of BC-qZSI is very small. The common mode current ripple of BC-qZSI can be seen Figure 11(d). The common mode current of BC-qZSI also very small that has 1 mA peak to peak. From Figure 11, the common mode of BC-qZSI is better than conventional qZSI.

IV. Conclusion

In principle, CMV problems occur when the converter is isolated with galvanic material. If the inverter operates with a high switching frequency, the CMV also has a high frequency. High CMV leads to a high capacitive leakage current returning to the source due to the interaction between the high rate of change of the CMV and the inherent leakage capacitance. This can cause undesirable situations, such as tripping nuisance ground current protection. Apart from the CMV issue, the conventional VSI is also limited because its output voltage cannot exceed the input voltage. This paper proposes the combination of a qZSI with a bidirectional converter (BC), called BC-qZSI. In this single-stage configuration, the voltage gain (output voltage higher than input voltage) is provided by the quasi-Z-source network, while the BC functions as an active filter to reduce CMV. This BC-qZSI topology offers significant advantages, including high output voltage, a high-quality sinusoidal output (achieving a THD_v of 2 %), and the elimination of the need for an additional output filter. The continuous input current is also maintained, minimizing system losses. The proposed inverter is verified by mathematical analysis and simulation using PSIM software. The simulation results show that the BC-qZSI output voltage is 261.7-volt peak or 185 Vrms, and the CMV and current are significantly lower than the conventional qZSI.

Declarations

Author contribution

All authors contributed equally as the main contributor of this paper. All authors read and approved the final paper.

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Competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The use of AI or AI-assisted technologies

No AI or AI-assisted technologies were used in the preparation of this manuscript.

Additional information

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