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A new multilevel buck-boost inverter structure using seven active switches

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Abstract

Generally, multilevel inverters function as voltage step-down or step-up converters. This paper discussed a new type of multilevel inverter, specifically five-level and seven-level designs that use seven active switches, which can increase or decrease the output voltage. The first study on using equal DC sources (E + E), known as symmetric, in the five-level setup for adjusting voltage was conducted, and then it was expanded to seven levels using an uneven DC source (2E + E), called asymmetric, with a new control method that works differently for each function. This multilevel voltage step-up (boost) and step-down (buck) inverter fundamentally has two components: a DC voltage level generator and a voltage step-up and polarity generator. This work provides a detailed look at how the multilevel voltage boost and buck inverter is built to show the features of the suggested design. Simulation data is provided to confirm how well each proposed design works with five-level and seven-level voltage increases and decreases in an inverter, using the sinusoidal pulse-width modulation (PWM) index and PWM duty cycle for better understanding. By the simulation, the total harmonic distortion (THD) value of the inverter when it operates as a buck is 1.26-1.32 %, and when it operates as a boost, it is 1.32-1.36 %. These values are still below 5 % in accordance with IEEE 519 standards and demonstrate a unity power factor.

Keywords: buck-boost inverter; five-level inverter; multilevel inverter; seven-level inverter.

I. Introduction

An inverter is a device that converts energy from DC to AC, widely used in electronic devices and commonly found in renewable energy systems, electric motor drives, etc. To improve the performance of inverters, many multilevel inverter topologies have been developed due to the numerous advantages they offer. Researchers have studied and advanced multilevel inverter topologies in recent decades, applying them in various types of homes, businesses, and factories. Multilevel inverters exhibit superior power quality relative to traditional two-level inverters [1][2]. The decrease in harmful electrical noise, the wave shape being more like a smooth sine wave, and the lower pressure on the switch have made it much easier to use. Multilevel inverters are employed in many areas of electrical engineering for low and medium-voltage/power applications, including renewable energy systems, distributed generation systems,

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industrial drive applications, and uninterruptible power supplies, among others [3][4][5]. A multilevel inverter has multiple active and passive power semiconductor devices, along with filters, coupled to a DC voltage source to provide a staircase waveform that closely matches a sinusoidal output, thereby reducing the size of the filters employed.

The following is a comprehensive review based on the AC output voltage remaining lower than the DC input voltage and the complexity of multilevel inverter configurations, as well as the excessive number of switches and high switching frequencies. Many symmetric and asymmetric multilevel inverters are unable to produce an AC output voltage that exceeds the DC input voltage. Researchers have studied five-level inverters with automatic balancing capacitors, but the AC output voltage remains lower than the DC input voltage [6][7][8]. The seven-level inverter with an automatic balancing capacitor also makes an AC output voltage that is still lower than the DC input voltage [9][10][11]. Additionally, the seven-level inverter that uses an asymmetric DC source (with voltages E and 2E) also produces an AC output voltage that is lower than the DC input voltage [12][13][14]. On the other hand, several topologies have successfully achieved higher AC output voltages, including five-level inverters [15][16][17], and seven-level inverters [18][19][20], where the AC output voltage exceeds the DC input voltage. Nevertheless, the condition of lower AC output voltage remains common and is a major limitation. The complexity of each configuration, whether operating in buck or boost mode, is always directly correlated with the challenges in active switching control methods for generating the appropriate voltage. Symmetrical multilevel inverters always have a more complex variation of switching pattern combinations to maintain voltage balance on the capacitors, thus resulting in increased control complexity [21][22][23]. Asymmetrical multilevel inverter configurations are used for higher output levels with the same number of components [24][25][26], but they also have the consequence of complex control. New inverters, such as those using connected inductors [27] or inductor-diode booster units [28], yield excellent results but with complexity due to current control mechanisms. Five-level type-F inverters offer benefits such as lower switching voltage and losses, but they require a balancing circuit using a buck-boost converter to maintain the DC-link capacitor voltage, which adds further complexity [29]. The three-level architecture that combines a type-T multilevel inverter with a boost converter has limits in capacitor voltage balancing and cannot be completely categorized as a single-stage inverter [30]. Researchers consistently identify the large number of switches and the high frequency of switching as severe problems. The symmetric design multilevel inverters require more switches, gate driver circuits, and DC voltage sources, which leads to increased size, cost, and control complexity [21][22][23]. The new five-level design, although it uses a smaller number of capacitors and switches than the two-stage boost converter, still suffers from the major problem of “excessive number of switches and high-frequency switching” [31]. The capacitor-switch structure is compact and can generate nine voltage levels from one source and two capacitors, but it employs twelve switches and requires independent pulse control for each switch [32]. The five-level bidirectional converter for battery charging requires many switches and independent pulse control, which are detrimental to its practical realization [33]. Finally, the five-level boost-buck inverter was explored and produced utilizing ten active power switches, and the essential factor that should be regarded is the number of active power switches employed [34]. According to the above description, a table can be created regarding a comparative analysis between the proposed inverter and previously reported multilevel inverter structures in terms of switch count, voltage gain, and THD performance, as shown in Table 1.

It is clear from the previously mentioned description that the research gaps comprise an increase in the number of active power switches, which is associated with a heightened complexity in the control strategy in multilevel systems. Additionally, the system must be capable of operating as a buck-boost inverter, which is a type of power converter that can step up or down voltage levels, and it must satisfy the IEEE THD

Table 1.
Multilevel inverter structures in terms of switch count, voltage gain, and THD performance.

Level Inverter	Reference	Switch Count	Voltage Gain	THD
Two-level inverters	[1]-[5]	4	Step down	High
Five-level inverter	[6]-[8]	6 to 8	Step down	Low
Seven-level inverter	[9]-[14]	8	Step down	Low
Five-level inverter	[15]-[17]	8	Step up	Low
Seven-level inverter	[18]-[20]	8	Step up	Low
Five-level inverter	[27][29][30][33][34]	8 to 12	Step up-down	Low

standard of 5 %. This paper examines a multilevel buck-boost inverter that utilizes seven active power switches. The paper outlines the five-level and seven-level topologies, detailing their characteristics under both symmetric and asymmetric input voltages. The control strategy is formulated by analyzing the potential operating modes. It is noted that the control strategies for both five-level and seven-level systems exhibit similarities, allowing for the application of the same control to both five-level and seven-level buck-boost inverters. The objective of this paper is to minimize the number of power semiconductor devices and symmetric (E + E) and asymmetric (2E + E) DC voltage sources in five-level and seven-level buck-boost inverter applications. The control strategies of each will vary depending on the operating modes that occur within a single cycle and must always comply with the IEEE 519 standard, which includes THD and power factor. The paper is organized as follows: Section II provides details on the design of the symmetric five-level buck-boost inverter and the asymmetric seven-level buck-boost inverter, along with their operating modes and control systems. The proposed multilevel inverter is the subject of Section III, which presents the simulation results and discussion. Section IV develops conclusions from the simulation results.

II. Materials and Methods

Figure 1 illustrates the proposed new buck-boost multilevel inverter topology. It comprises an inductor, a non-polar capacitor, a resistive load, and two passive switches (D1-D2), in addition to seven active switches (insulated-gate bipolar transistor (IGBT) without parallel diode) (IG_1–IG_6 and IG_B). The IGBTs (IG_1–IG_2) establish levels on the DC voltage side, while the IGBT (IG_B) functions as a voltage booster and is outfitted with a positive and negative polarity inverter at the frequency of the electrical grid, IGBTs (IG_3-IG_6) In Figure 1(a), a five-level buck-boost inverter is formed when the DC voltage has the same magnitude (symmetric), while a seven-level buck-boost inverter is formed when the DC voltage has various magnitudes (asymmetric), despite having the same basic configuration.

Figure 1(a) illustrates the side that is accountable for generating the three-level voltage of the DC-DC converter. The potential operating modes are depicted in Figure 2. It illustrates four distinct operating modes: Mode 1: IG_1 and IG_2 are conducting, while D1 and D2 are not conducting, resulting in an output voltage (V_{DC-DC}) of 2E. Mode 2: IG_1 and D2 are conducting, while D1 and IG_2 are not conducting, resulting in an output voltage (V_{DC-DC}) of E. Mode 3: IG_2 and D1 are conducting, while IG_1 and D2 are not conducting, resulting in an output voltage (V_{DC-DC}) of E. Mode 4: D1 and D2 are conducting, while IG_1 and IG_2 are not conducting, resulting in an output voltage (V_{DC-DC}) of 0. The output voltage (V_{DC-DC}) exhibits three distinct levels, specifically 2E, E, and 0.

The high-voltage side achieves this by activating IG_B, facilitating a rapid increase in the inductor's current. The switching frequency in this mode is exceedingly high, guaranteeing optimal operation of the voltage booster, Figure 3(a). During the polarity reversal, IG_3 and IG_6 operate in the positive cycle, Figure 3(b), while IG_4 and IG_5 function in the negative cycle, Figure 3(c). Consequently, the output will oscillate between positive, and negative values, generating an AC voltage with a frequency of 50 Hz, consistent with the operational frequencies IG_3 = IG_6 and IG_4 = IG_5. The specific operational modes are illustrated in Figure 3. Table 2 shows a summary of the operating modes that occur in the five-level buck-boost inverter, where "1" indicates the power switch is conducting and "0" indicates the power switch is not conducting.

Figure 1(b) illustrates the side that is accountable for generating the four-level voltage of the DC-DC converter. The potential operating modes are depicted in Figure 4. It illustrates four distinct operating modes: Mode 1: IG_1 and IG_2 are conducting, while D1 and D2 are not conducting, resulting in an output voltage

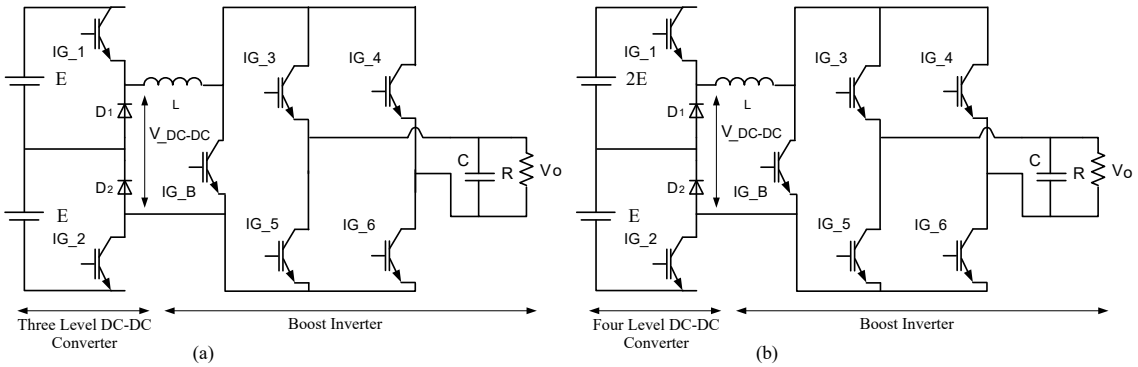

Figure 1. Buck-boost multilevel inverter: (a) Five-level, (b) Seven-level.

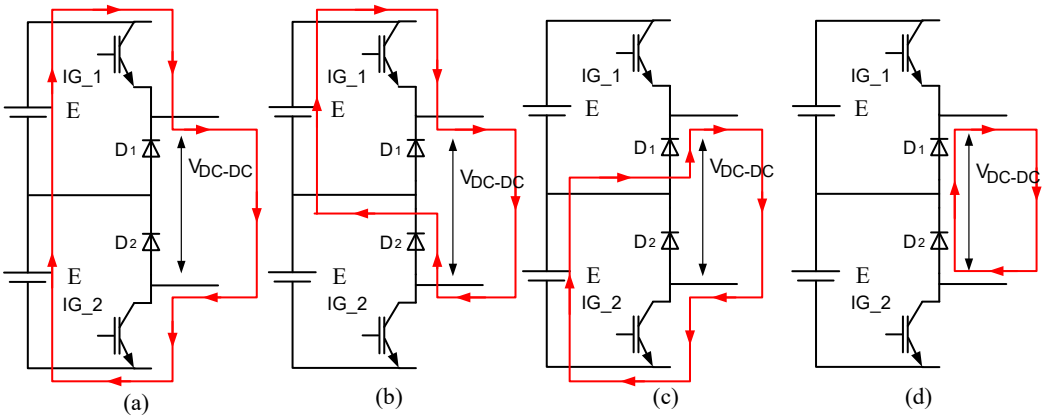

Figure 2. Three-level DC-DC converter operation mode: (a) Mode 1; (b) Mode 2; (c) Mode 3; and (d) Mode 4.

(V_{DC-DC}) of 3E, Figure 4(a). Mode 2: IG_1 and D2 are conducting, while D1 and IG_2 are not conducting, resulting in an output voltage (V_{DC-DC}) of 2E, Figure 4(b). Mode 3: IG_2 and D1 are conducting, while IG_1 and D2 are not conducting, resulting in an output voltage (V_{DC-DC}) of E, Figure 4(c). Mode 4: D1 and D2 are conducting, while IG_1 and IG_2 are not conducting, resulting in an output voltage (V_{DC-DC}) of 0, Figure 4(d). The output voltage (V_D) exhibits four distinct levels, specifically 3E, 2E, E, and 0.

The identical approach is implemented on the high-voltage side, as illustrated in Figure 4. A summary of the operating modes that occur in the seven-level buck-boost inverter is presented in Table 3. The power switch is conducting when "1" is present, and it is not conducting when "0" is active. Table 2 and Table 3 show that the five-level buck-boost inverter with voltage sources E and E, and the seven-level buck-boost inverter with voltage sources E and 2E work the same way, but they give different output values.

The output voltage (V_{DC-DC}) equation against the input voltage (V_i: E, E; 2E, E) for five-level and seven-level inverters is shown in the following equation (1):

$$V_{DC-DC} = I_{nd}\, V_i \tag{1}$$

where I_{nd} is the modulation index of the sinusoidal pulse width. The output voltage (V_o) equation against the input voltage (V_{DC-DC}) for boost inverters is shown in the following equation (2):

$$V_o = \frac{1}{1-D_{cy}} V_{DC-DC} \tag{2}$$

where D_{cy} is the duty cycle of the pulse-width modulation (PWM). The following is the generic equation (3) for the output voltage of the five-level and seven-level buck-boost inverters:

$$V_o = \frac{I_{nd}}{1-D_{cy}} V_i \tag{3}$$

A very high switching frequency will make the AC waveform look like a changing DC waveform on both the positive and negative sides, depending on the

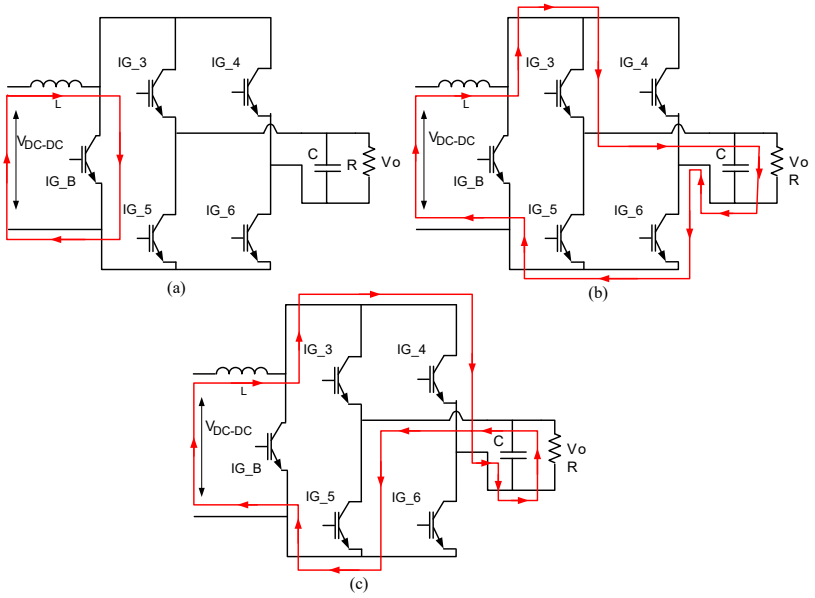

Figure 3. AC-AC boost operation mode: (a) Mode 1; (b) Mode 2; and (c) Mode 3.

Table 2.
Five-level buck-boost inverter operation mode.

IG_1	IG_2	D1	D2	IG_B	IG_3	IG_4	IG_5	IG_6	Vo
1	1	0	0	1/0	1	0	0	1	+2E
1	0	0	1	1/0	1	0	0	1	+E
0	1	1	0	1/0	1	0	0	1	+E
0	0	1	1	1/0	1	0	0	1	0
1	1	0	0	1/0	0	1	1	0	-2E
1	0	0	1	1/0	0	1	1	0	-E
0	1	1	0	1/0	0	1	1	0	-E
0	0	1	1	1/0	0	1	1	0	0

voltage-boosting mode used to create the AC waveform. The magnitude of the output current disturbance (ΔI) can be determined using equation (4), where f is the frequency IG_B:

$$\Delta I = \frac{V_D D_{cy}}{Lf} \quad (4)$$

This frequency is much more important for control and will greatly reduce the need for filters on the output side, since the boost voltage operates at a significantly higher switching frequency. The magnitude of the disturbance in the output voltage (ΔV) is determined by the following equation (5):

$$\Delta V_C = \frac{I_O D_{cy}}{Cf} \quad (5)$$

The control strategy for both converters is identical, as seen from the existing operating modes, detailed in Figure 2 and Figure 4. The logic gate equations for controlling IG_1 and IG_2 based on Table 2 and Table 3 are obtained as equation (6) and equation (7):

$$IG_1 = C + B \quad (6)$$

$$IG_2 = A \oplus B + C \quad (7)$$

In this context, A, B, and C refer to levels of sinusoidal PWM generators. Note that for the five-level buck-boost inverter, only A and B are used, while C is ignored. Figure 5 illustrates the control strategy for output voltage in five-level and seven-level buck-boost inverters. This paper concentrates on inverter topology, thus omitting discussions on proportional and integral controller strategies. Figure 6 illustrates the output voltage control algorithm for buck-boost inverters with five and seven levels. The absolute sinusoidal PWM process is used to control switches IG_1 and IG_2, and it is compared with a triangular carrier signal at the phase level. The voltage is increased in the PWM component by activating IG_B, and polarity is established at the zero-crossing detector's end by adjusting switches IG_3-IG_6. This procedure would ensure that the output voltage consistently aligns with the intended voltage (V_ref). The voltage control process will show that the buck-boost inverters with five and seven levels, which were built with different ways to operate for a control strategy, support the results seen in the simulations mentioned in section 3.

III. Results and Discussions

The new five-level and seven-level buck-boost inverter designs are evaluated for their ability to generate the required output voltage using Power Simulator software. The experiments are conducted using the setup depicted in Figure 5, the control strategy, and the algorithm control depicted in Figure 6.

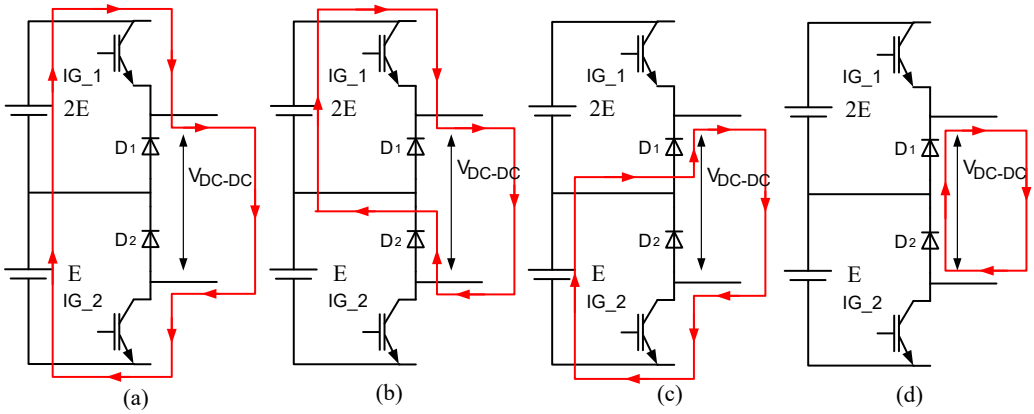

Figure 4. Four-level DC-DC converter operation mode: (a) Mode 1; (b) Mode 2; (c) Mode 3; and (d) Mode 4.

Table 3.
Seven-level buck-boost inverter operation mode.

IG_1	IG_2	D1	D2	IG_B	IG_3	IG_4	IG_5	IG_6	Vo
1	1	0	0	1/0	1	0	0	1	+3E
1	0	0	1	1/0	1	0	0	1	+2E
0	1	1	0	1/0	1	0	0	1	+E
0	0	1	1	1/0	1	0	0	1	0
1	1	0	0	1/0	0	1	1	0	-3E
1	0	0	1	1/0	0	1	1	0	-2E
0	1	1	0	1/0	0	1	1	0	-E
0	0	1	1	1/0	0	1	1	0	0

Table 4 provides a comprehensive list of the parameters that are associated with the Power Simulator model. The Power Simulator software is employed in this paper for simulation purposes.

The software is used to check the test, and it is divided into two stages: five-level and seven-level buck-boost inverters. The first step is to test the five-level buck-boost inverter with an output voltage control block (Figure 5) and a control method (Figure 6) that works with voltages E and E. In Figure 7, you can see how IG_1 and IG_2 switch on and off, as well as the three-level DC-DC converter's output voltage, which is set to 200 V, 100 V, and 0 V. This scenario means that the plan to create three types of DC voltage can be shown to work. As shown in Figure 8, the next step is to change IG_3–IG_6 and test how IG_B switches on and off and how positive and negative polarities form. The switching pattern has happened, and IG_3 and IG_6 are used to make the positive polarity reverse pattern happen. IG_4 and IG_5 are used to make the negative polarity pattern happen.

The output voltage side of the five-level buck-boost inverter was tested under buck conditions, which is a condition in which the output voltage is lower than the input voltage. The five-level buck-boost inverter's output voltage is below 200 V (E + E), as demonstrated in Figure 9. Consequently, it is capable of functioning as a buck inverter. The image also demonstrates that the waveform of the current and voltage has a unity power factor and a THD of 1.26 %. This simulation result indicates that the five-level buck-boost inverter can function as intended.

Advanced testing for boost inverter conditions, which is a condition in which the output voltage is higher than the input voltage. The five-level buck-boost inverter's output voltage is above 200 V (E + E), as demonstrated in Figure 10. Consequently, it is capable of functioning as a boost inverter. The image also demonstrates that the waveform of the current and voltage has a unity power factor and a THD of 1.32 %. This simulation result indicates that the five-level buck-boost inverter can function as intended.

Table 4.
Simulation parameters.

Parameters	Value
Input voltage E	100 V
Inductor	2 mH
Capacitor	10 uF
SPWM switching	5 kHz
PWM switching	20 kHz
Proportional (K_p)	0.5
Integral (Tis)	0.003
Resistive load	10 Ω

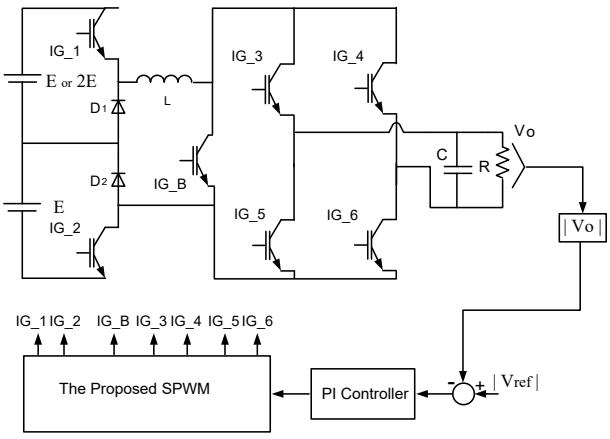

Figure 5. Voltage control strategy for buck-boost inverters with five and seven levels.

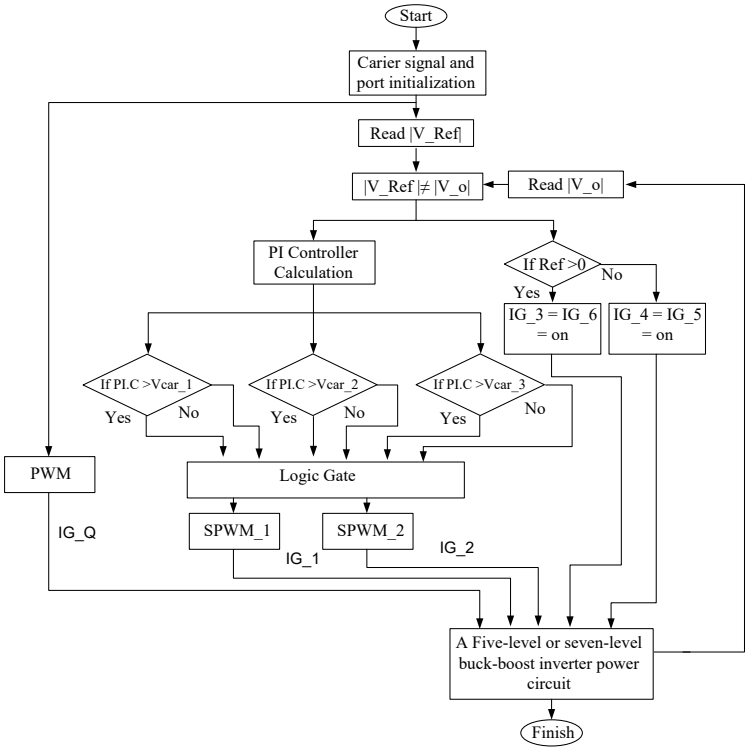

Figure 6. Proposed control modulation strategy for buck-boost inverters with five and seven levels.

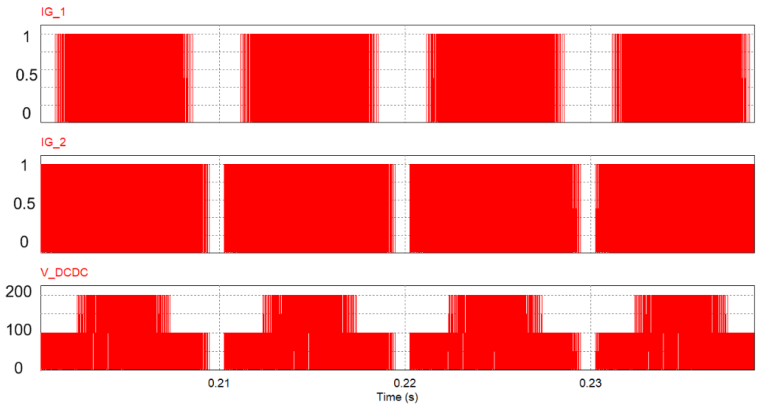

Figure 7. Switching Pattern IG_1; IG_2; and three-level DC.

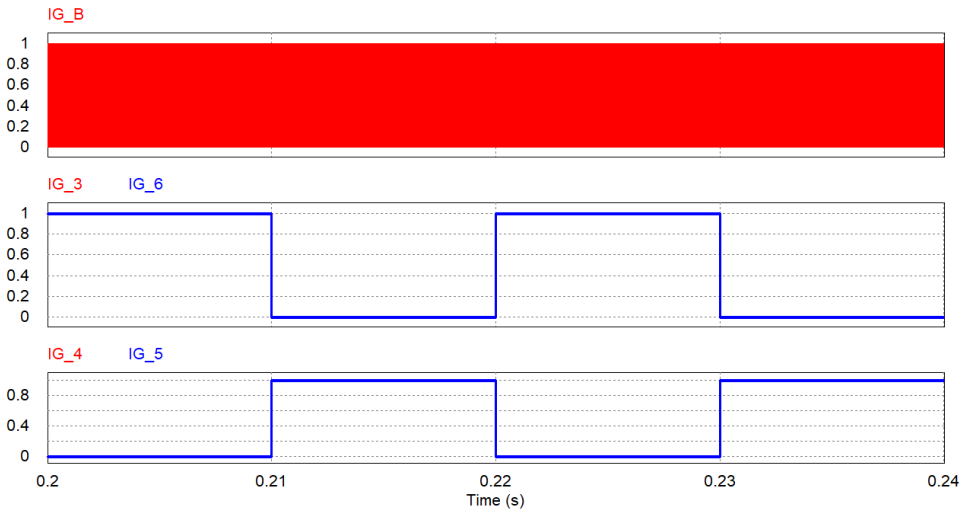

Figure 8. Switching Pattern IG_B; IG_3 = IG_6; and IG_4 = IG_5.

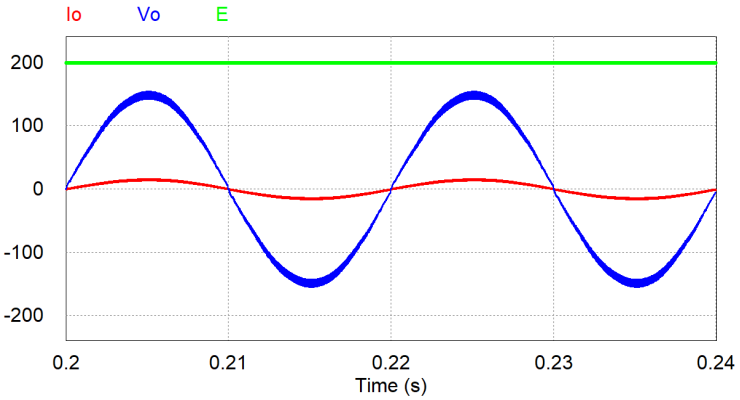

Figure 9. Five-level buck-boost inverter under buck condition.

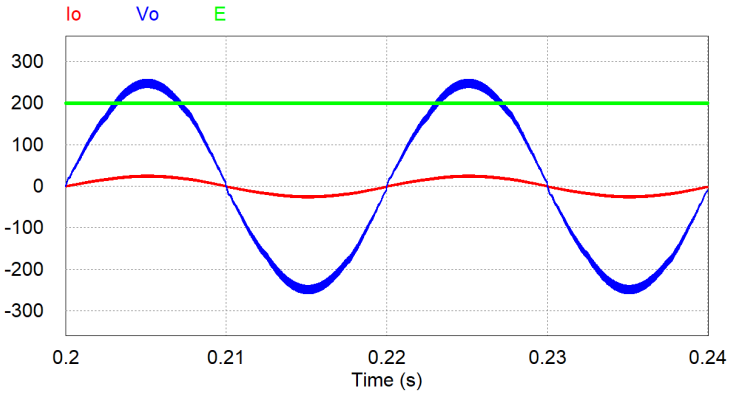

Figure 10. Five-level buck-boost inverter under boost condition.

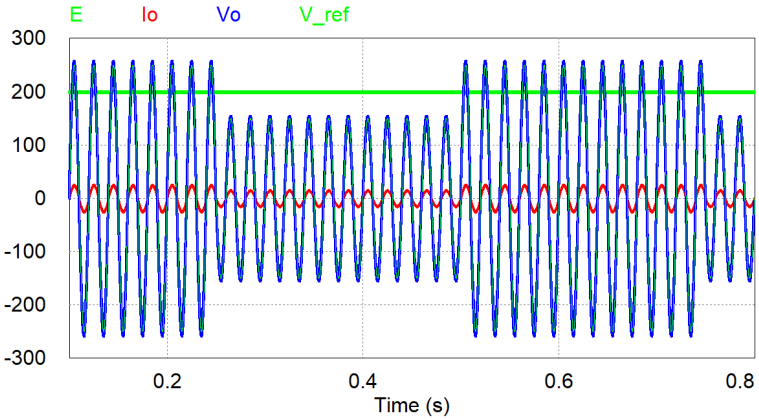

Figure 11. Output voltage response of five-level buck-boost inverter.

The five-level buck-boost inverter's final stage testing is performed using a variable reference voltage that satisfies the buck and boost methodologies on the inverter output voltage side, Figure 11. It is evident that the output voltage (V_o) will consistently adhere to the reference voltage (V_ref). In this scenario, the output voltage (V_o) may occasionally exceed the input voltage of 200 V (E + E) and, conversely, may fall below the input voltage. Consequently, it can be inferred that the five-level buck-boost inverter that has been analyzed and simulated is functioning as anticipated.

The second stage involves checking the seven-level buck-boost inverter, which has a controlled output voltage system shown in Figure 5, and a control method shown in Figure 6, using input voltages E and 2E. Figure 12 displays the output voltage of the four-level DC-DC converter, which can generate 300 V, 200 V, 100 V, and 0 V, along with the switching patterns of IG_1 and IG_2. Consequently, the feasibility of the control strategy to establish four levels of DC voltage can be demonstrated. The next step is to change IG_3-IG_6, as shown in Figure 13, to check the switching pattern of IG_B and create positive and negative voltages. The switching pattern has been observed, and the positive polarity reversal pattern is obtained by activating IG_3 and IG_6, while IG_4 and IG_5 are employed for negative polarity.

The assessment of the seven-level buck-boost inverter on the output voltage side was done while it was in buck mode, meaning the output voltage is lower

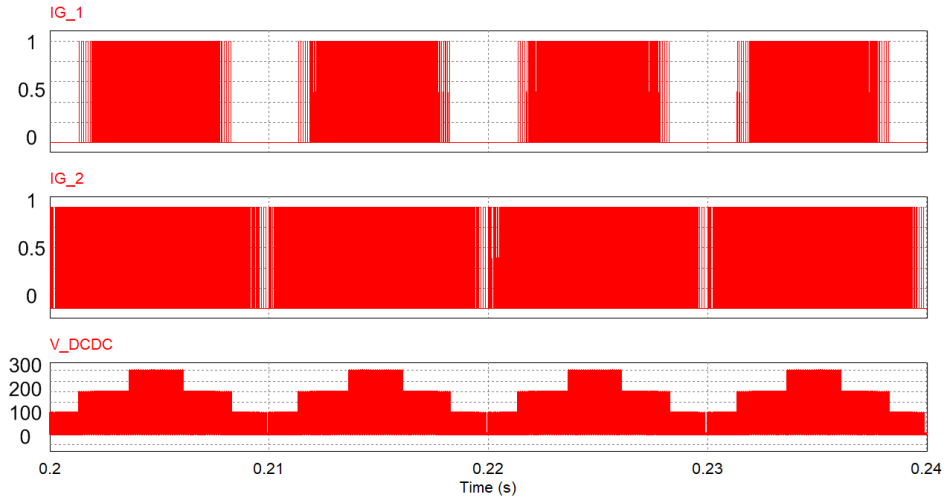

Figure 12. Switching Pattern IG_1; IG_2; and four-level DC.

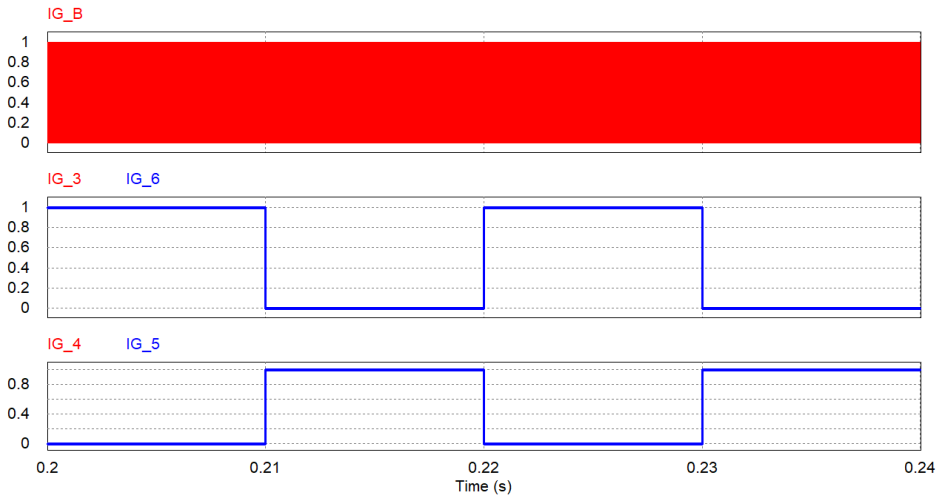

Figure 13. Switching Pattern IG_B; IG_3 = IG_6; and IG_4 = IG_5.

than the input voltage. Figure 14 illustrates that the output voltage of the seven-level buck-boost inverter is below 300 V (2E + E), thereby confirming that it functions effectively as a buck inverter. The graphic indicates that the current and voltage waveforms exhibit a unity power factor and a THD of 1.28 %. The simulation results indicate that the seven-level buck-boost inverter functions effectively as intended.

The next assessment of the seven-level buck-boost inverter on the output voltage side was done while it was in boost mode, meaning the output voltage is higher than the input voltage. Figure 15 illustrates that the output voltage of the seven-level buck-boost inverter is above 300 V (2E + E), thereby confirming that it functions effectively as a boost inverter. The graphic indicates that the current and voltage waveforms exhibit a unity power factor and a THD of 1.36 %. The simulation results indicate that the seven-level buck-boost inverter functions effectively as intended.

The seven-level buck-boost inverter's final stage testing is performed using a variable reference voltage that satisfies the buck and boost methodologies on the inverter output voltage side, Figure 16. It is evident that the output voltage (V_o) will consistently adhere to the reference voltage (V_ref). In this scenario, the output voltage (V_o) may occasionally exceed the input voltage of 300 V (2E + E) and, conversely, may fall below the input voltage. Consequently, it can be inferred that the seven-level buck-boost inverter that has been analyzed and simulated is functioning as anticipated.

The simulation findings indicate that both the five-level and seven-level buck-boost inverters function effectively as intended. Five-level and seven-level buck-boost inverters utilize an identical quantity of power switches, specifically seven active power switches, with an input voltage of (E + E) for five levels and (2E + E) for seven levels. The control strategy for both five-level and seven-level buck-boost inverters is the same because they work similarly and have a similar design, with the only difference being the input voltage. The simulation findings indicate that the designed and simulated five-level or seven-level buck-boost inverter operates as expected. The THD of the output voltage in

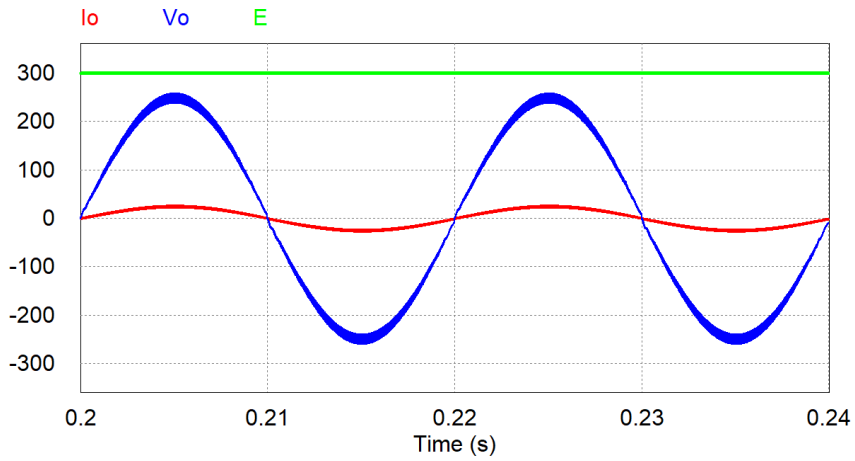

Figure 14. Seven-level buck-boost inverter under buck condition.

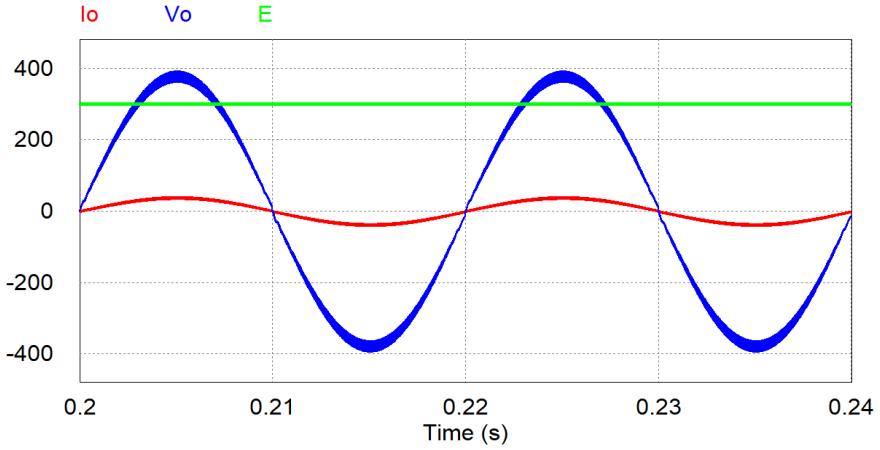

Figure 15. Seven-level buck-boost inverter under boost condition.

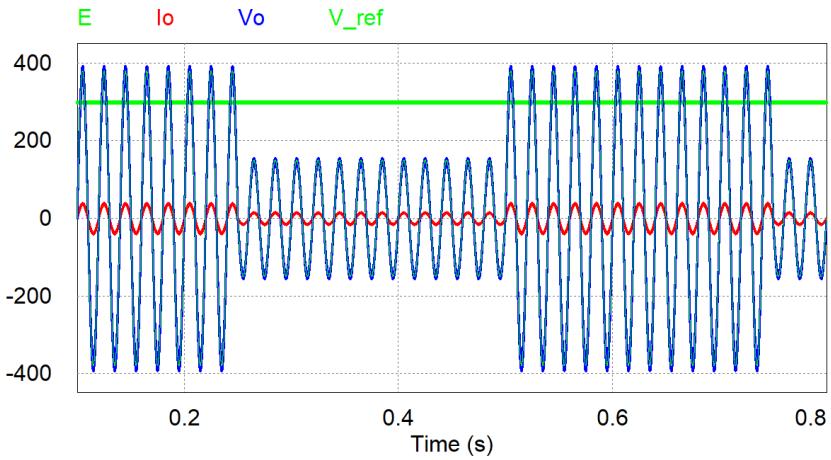

Figure 16. Output voltage response of seven-level buck-boost inverter.

both the simulation and hardware tests meets the IEEE 519 standard, with values always staying below 5 % [35][36]. Both five-level and seven-level buck-boost inverters can be improved to higher levels by changing how the multi-level DC waveform is created, using either a symmetric or asymmetric method. It's important to note that using a symmetric method will require more power switches in the inverter design, while an asymmetric method will need fewer switches. However, the balance of input power must be considered and managed carefully. It is important to recognize that employing a symmetric technique will lead to the inverter configuration incorporating numerous power switches, whereas an asymmetric strategy will utilize far fewer power switches. Nonetheless, the equilibrium of input power must be taken into account and necessitates meticulous management.

A new multilevel inverter has been developed based on various operating modes to generate a new control strategy, which has been verified through computational simulations and demonstrated good

performance. The following recommended step for further verification is hardware implementation, where the simulation results serve as a reference for the success of the implementation. Furthermore, this multilevel inverter can be applied to renewable energy systems, such as photovoltaic systems. The integration of the maximum power tracking algorithm to the AC-AC boost inverter controller is used to achieve better performance and simplicity in terms of topology and control systems.

IV. Conclusion

A new multilevel (five-level and seven-level) buck-boost inverter that has been studied for its operating modes and control strategies can work well. With the same control strategy, both can function as boost inverters and buck inverters. The five-level and seven-level buck-boost inverter topologies each have seven active power switches. The only difference is in the input voltage usage, which is E + E for the symmetric five-level and 2E + E for the asymmetric seven-level. Based on simulation experiments, the THD value of the inverter when it operates as a buck is 1.26-1.32 %, and when it operates as a boost, it is 1.32-1.36 %. These values are still below 5 % in accordance with IEEE 519 standards and demonstrate a unity power factor. This multilevel buck-boost inverter is suitable for new and renewable energy applications.

Declarations

Author contribution

Leonardus Heru Pratomo: Conceptualization, Formal analysis, Investigation, Visualization, Supervision, Data Curation, Software, Writing – original draft, Writing – review & editing, Corresponding author. **Florentinus Budi Setiawan**: Resources, Funding acquisition, Writing – review & editing. **Sushil Paudel**: Resources, Software, Writing – review & editing. All authors have read and agreed to the published version of the manuscript.

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Competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The use of AI or AI-assisted technologies

During the preparation of this work, the authors used Power Simulator software to simulate the proposed model, QuillBot to check the grammar, and Turnitin to check for similarity. After using these tools, the authors reviewed and edited the content as needed and took full responsibility for the content of the publication.

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