Journal of Mechatronics, Electrical Power, and Vehicular Technology 16 (2025) 256-265

Journal of Mechatronics, Electrical Power, and Vehicular Technology

e-ISSN: 2088-6985
p-ISSN: 2087-3379

mev.brin.go.id

Design and implementation of a DC-DC buck converter with Type III compensator control

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Abstract

This paper presents a low-cost hardware realization of a Type III compensated DC–DC buck converter with experimental validation under practical load conditions. The compensator is designed using MATLAB Bode plot analysis to achieve the target phase margin, and the resulting pole–zero configuration is verified through LTspice simulation before implementation on a microcontroller-based hardware prototype. Performance testing is conducted under both resistive and DC motor loads to evaluate improvements over an open-loop configuration. Experimental results show that the proposed closed-loop design significantly accelerates transient recovery, reducing settling time from 85–134 ms in the open-loop system to 0.39–5.2 ms in the compensated system, representing improvements of up to two orders of magnitude depending on the load. The closed-loop converter also achieves tighter steady-state regulation around 6 V and smaller effective voltage dips during load transients, confirming the effectiveness of the Type III compensator in enhancing both dynamic and steady-state performance. The implementation demonstrates a practical and cost-efficient approach for applying Type III compensation on low-cost hardware platforms suitable for educational and prototype-level power electronics applications.

Keywords: buck converter; Bode plot; phase margin; transient response; Type III compensator.

I. Introduction

Electric energy plays a vital role in modern life, particularly in powering electronic devices that enhance human activities and productivity. Most electronic systems require a stable direct current (DC) power supply capable of maintaining voltage regulation under varying input conditions and load demands [1][2]. The required DC voltage levels differ across applications, creating the need for efficient power conversion devices that can step down or step up DC voltages, commonly known as DC–DC converters [3][4].

A buck converter is a widely used DC–DC power converter that produces an output voltage lower than its input voltage, with applications ranging from small household electronics to large industrial equipment [5]. Its operation is based on controlling a metal-oxide-semiconductor field-effect transistor (MOSFET) that alternates between on and off states through a pulse

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https://doi.org/10.55981/j.mev.2025.1321

Received 6 November 2025; revised 5 December 2025; accepted 10 December 2025; available online 27 December 2025; published 31 December 2025

How to Cite: Fahmizal *et al.*, "Design and implementation of a DC–DC buck converter with Type III compensator control," *Journal of Mechatronics, Electrical Power, and Vehicular Technology*, vol. 16, no. 2, pp. 256-265, Dec. 2025.

width modulation (PWM) signal [6][7]. During the on-state, current flows from the source through the MOSFET to the inductor and load. During the off-state, the MOSFET turns off, and the inductor continues supplying current to the load through the freewheeling diode and output capacitor, ensuring continuous energy transfer.

To maintain output voltage stability, a control system is essential [8]. Two common control approaches are open-loop and closed-loop systems [9]. The open-loop system lacks feedback, making it unable to correct deviations in output voltage, whereas the closed-loop system employs feedback to detect errors and adjust the control signal accordingly, resulting in improved voltage regulation and transient response. Consequently, open-loop control is rarely used in practical applications.

Various control methods have been applied to buck converters, including proportional–integral–derivative (PID) controllers [10][11], linear quadratic integrator (LQI) [12], sliding mode control (SMC) [13], model predictive control (MPC) [14][15], and compensator-based designs [16]. PID controllers are simple to implement but may struggle to compensate for the double-pole resonance introduced by the inductor–capacitor network which can lead to low phase margin and oscillatory behavior. LQI improves steady-state accuracy and can handle multi-objective control but it requires an accurate state-space model and involves matrix computations that increase implementation complexity especially for low-cost microcontrollers. SMC offers robustness to disturbances and parameter variations but introduces design complexity and may generate high-frequency switching noise. MPC provides excellent transient performance and constraint handling, yet it demands intensive real-time computation and precise system modeling, making it less suitable for low-power or resource-constrained embedded applications.

Type III compensators have become an industry standard for voltage-mode controlled buck converters operating at fixed switching frequencies because they directly address the double-pole resonance of the LC filter, allow high loop bandwidth, and maintain low output ripple, while remaining simpler to implement than advanced nonlinear methods such as SMC [17]. They can provide up to 180° of phase boost, ensuring stability at higher crossover frequencies and enabling faster transient response without sacrificing steady-state performance.

Reference [17] presents a digitally implemented Type III compensator designed to improve dynamic performance but its focus remains on small-signal analysis and theoretical pole–zero placement for fast response. Similarly, Nagar *et al.* [18] design and analyse a Type III compensator for a buck converter but limit their evaluation to simulations, without validating the design on real hardware. Neither study investigates microcontroller-based implementation, switching behaviour under practical conditions, or the real-time performance of the converter under varying loads. These limitations create a gap that the present study addresses by implementing a microcontroller-controlled buck converter, performing hardware validation, and analysing the converter's performance under both resistive and inductive load conditions.

In this study, a Type III compensator is designed using MATLAB Bode plot analysis to achieve the desired phase margin. The design is validated through LTspice simulations, where passive component values are determined based on the calculated phase margin. The configuration demonstrating stability and minimal steady-state error is then implemented on a physical buck converter and evaluated under various load conditions, including resistive and DC motor loads, to quantify its performance improvements over an open-loop configuration.

II. Materials and Methods

Figure 1 illustrates the overall workflow used in this study. The process begins with a literature review to identify recent developments in Type III compensator design for buck converters. Next, the buck-converter model is developed to support the design of the Type III compensator. In the following step, LTspice

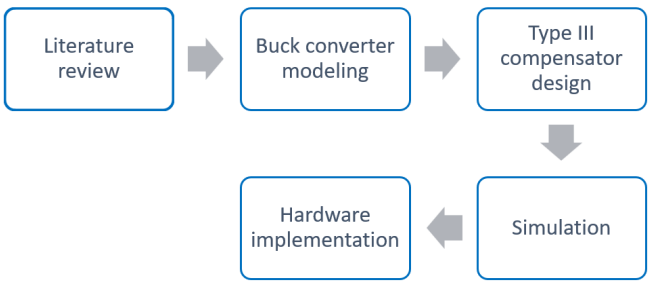

Figure 1. Study workflow.

simulations are performed to verify the small-signal behavior and to validate the appropriate pole–zero placement and phase-margin requirements of the compensator. Once the compensator design is validated in simulation, the parameters are implemented in the hardware prototype, and all performance testing is carried out on the physical buck-converter system under resistive and DC-motor loads.

A. Buck converter model

The state-space matrix equation involves state variables associated with components that store energy, namely, the inductor and capacitor [19]. Based on the analysis of the buck converter circuit using Kirchhoff's Voltage and Current Laws, the matrix variables in the state-space equation can be transformed into state matrix values and output equations. For the on-state and off-state conditions of the buck converter, the equations can be represented as equation (1),

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{1}$$

where $x(t)$ is the state vector containing the inductor current and capacitor voltage, A is the system matrix representing the internal dynamics of the buck converter, B is the input matrix that relates the input voltage or switch state to the system, and $u(t)$ is the control input applied to the converter.

State-space averaging is used to transform a nonlinear system, caused by the switching process, into a linear system. The state-space averaging model is obtained by combining the equations for the on-time and off-time conditions while taking into account the duty cycle. This combination of both conditions results in a linearized model that enables the analysis of system response under small disturbances, such as changes in input voltage or load, known as the small-signal model. In general, the state-space averaging equations that consider the duty cycle under steady-state conditions are represented as equation (2),

$$\bar{x}_{avg}(t) = \left[d(t)A_{on} + d'(t)A_{off}\right]x(t) + [d(t)B_{on} + d'(t)B_{off}]u(t) \tag{2}$$

where $d(t)$is the duty cycle, A_{on} and A_{off} are the system matrices for the switch ON and OFF intervals, respectively, and B_{on} and B_{off} are the corresponding input matrices. The system output in the state-space averaging model, taking into account the duty cycle under steady-state conditions, is represented by the following equation (3),

$$V_{out_{avg}}(t) = \left[d(t)V_{out_{on}}(t) + d'(t)V_{out_{off}}(t)\right] \tag{3}$$

where $V_{out,on}$ and $V_{out,off}$ denote the output voltage expressions during the ON and OFF states. These averaged equations describe the linearized small-signal model obtained from state-space averaging.

Several parameter values of the buck converter are subjected to small-signal perturbations under steady-state conditions to obtain linearization around the operating point. These include $\hat{d}(t)$ as the duty cycle perturbation, $\hat{v}_{out}(t)$ as the output voltage perturbation, $\hat{x}(t)$ as the state variable perturbation (comprising inductor current and capacitor voltage), and $\hat{u}(t)$ as the perturbation in the input voltage and the diode forward bias. The equations are given as equation (4) to equation (7),

$$d(t) = D_{cycle} + \hat{d}(t) \tag{4}$$

$$V_{out}(t) = V + \hat{v}_{out}(t) \tag{5}$$

$$x(t) = X + \hat{x}(t) \tag{6}$$

$$u(t) = U + \hat{u}(t) \tag{7}$$

where $D_{cycle}, V, X,$ and U denote the steady operating point. Perturbations $\hat{d}$, $\hat{v}_{out}, \hat{x},$ and $\hat{u}$ are assumed to be small and products between perturbations are neglected.

The equations resulting from the addition of small-signal perturbations involve the multiplication of two parameters: the steady-state values and the perturbation variables, which leads to a second-order system. However, the product of small-signal perturbations can be neglected because their values are very small and have minimal impact on the overall equation. This simplification makes the system easier to linearize and analyze. The steady-state equation then becomes equation (8),

$$\frac{d(X+\hat{x}(t))}{dt} = A_{avg}X + B_{avg}U + A_{avg}\hat{x}(t) + B_{avg}\hat{u}(t) + \left[A_{on} - A_{off}\right]X\hat{d}(t) + \left[B_{on} - B_{off}\right]U\hat{d}(t) \tag{8}$$

By decomposing the parameter values of the state matrix, the following equation is equation (9) to equation (11),

$$A_{avg} = A_{on}D_{cycle} + A_{off}D'_{cycle'} \tag{9}$$

$$B_{avg} = B_{on}D_{cycle} + B_{off}D'_{cycle'} \tag{10}$$

$$C_{avg} = C_{on}D_{cycle} + C_{off}D'_{cycle'} \tag{11}$$

The averaged matrices $A_{avg}, B_{avg},$ and C_{avg} represent the linearized small-signal model of the converter obtained by weighting the ON and OFF state-space models according to the duty cycle. These averaged matrices are used for analyzing the converter dynamics around its operating point and for designing linear controllers such as the Type III compensator. The output voltage equation, after simplification by neglecting the multiplication of small-signal

perturbations in the second-order system, becomes equation (12),

$$V + \hat{v}_{out}(t) = C_{avg}X + C_{avg}\hat{x}(t) + \left[C_{on} - C_{off}\right]X\hat{d}(t) \quad (12)$$

Analysis of the system, particularly the state-space model of the buck converter, is used to describe the relationship between the input in the form of small variations in the duty cycle $\hat{d}(s)$ and the output in the form of variations in the output voltage $\hat{v}_{out}(s)$ in the Laplace domain. Based on the derived state equations and output voltage expression, a Laplace transformation is performed [18]. The resulting equations are as equation (13) to equation (14),

$$s\hat{x}(s) = A_{avg}\hat{x}(s) + \left[A_{on} - A_{off}\right]Xd(s) + \left[B_{on} - B_{off}\right]Ud(s) \quad (13)$$

$$\hat{v}_{out}(s) = C_{avg}\hat{x}(s) + \left[C_{on} - C_{off}\right]Xd(s) \quad (14)$$

The transfer function that uses the duty cycle as the input and the output voltage as the output yields the following equation (15),

$$\frac{\hat{v}_{out}(s)}{\hat{d}(s)} = C_{avg}\left[Is - A_{avg}\right]^{-1}\left(\left[A_{on} - A_{off}\right]X + \left[B_{on} - B_{off}\right]U\right) + \left[C_{on} - C_{off}\right]X \quad (15)$$

B. Type III compensator

The type III compensator consists of a system with two zeros and three poles, with one pole located at the origin. In frequency response control system design, it is necessary to determine the corner frequencies of the zeros and poles in the type III compensator circuit to understand when the effect of each zero or pole becomes significant on the Bode plot, both in terms of gain and phase [17]. One method that can be used to determine the corner frequencies of the zeros and poles is the K-factor method. The K-Factor method is one of the approaches used in the design of a Type III compensator, which places two zeros at the same corner frequency (ω_{zk}), and two poles at the same corner frequency (ω_{pk}). The system equation of the type III compensator using the K-Factor method approach is expressed as equation (16),

$$G_c(s) = H_c\frac{(s+\omega_{zk})^2}{s(s+\omega_{pk})^2} \quad (16)$$

The target phase margin (PM) at the gain crossover frequency ($\omega_{gain\ crossover}$) becomes the target in determining the corner frequencies of the zeros and poles in the Type III compensator control using the K-Factor method. The equation used in this determination process are as equation (17) to equation (21),

$$\phi_{boost} = \phi_{margin} - \phi G_p\left(j\omega_{gain\ crossover}\right) - 90° \quad (17)$$

$$K_{value} = tan^2\left(\frac{\phi_{boost}}{4} + 45°\right) \quad (18)$$

$$\omega_{zk} = \frac{\omega_{gain\ crossover}}{\sqrt{K_{value}}} \quad (19)$$

$$\omega_{pk} = \omega_{gain\ crossover} \cdot K_{value} \quad (20)$$

$$H_c = \frac{1}{\left|G_p\left(j\omega_{gain\ crossover}\right)G_c\left(j\omega_{gain\ crossover}\right)\right|} \quad (21)$$

The target PM (ϕ_{margin}) at the ($\omega_{gain\ crossover}$) is used to determine the required pole–zero placement of the type III compensator through the K-Factor method. First, the required compensator phase boost (ϕ_{boost}) is computed from the difference between the desired phase margin and the phase of the power-stage transfer function $G_p(s)$ at the crossover frequency, minus the inherent 90°phase lag of the integrator. The K-Factor value K_{value} is then obtained from the standard K-Factor expression, which determines the spacing between the compensator poles and zeros. Using this constant, the zero corner frequency (ω_{zk}) and pole corner frequency (ω_{pk}) are calculated symmetrically around ($\omega_{gain\ crossover}$). Finally, the compensator gain factor (H_c) is determined so that the magnitude of the product $G_p\left(j\omega_{gain\ crossover}\right)G_c\left(j\omega_{gain\ crossover}\right)$ becomes unity, ensuring that the loop gain crosses 0 dB at the desired frequency. In these equations, $\phi_{G_p}(j\omega_{gain\ crossover})$ represents the phase of the power-stage transfer function at crossover, ϕ_{boost} is the additional phase the compensator must provide, K_{value} is a design constant used to set pole–zero spacing, ω_{zk} and ω_{pk} are the compensator zero and pole frequencies, respectively, and H_c serves as the overall compensator gain adjustment.

Figure 2 depicts the circuit of the type III compensator. One of the components must be determined first before calculating the values of the other components, where the resistor R_2 is set to a value of 10 kΩ. The equations used to determine the passive component values in the type III compensator are as follows equation (22) to equation (26),

$$C_2 = \frac{1}{\omega_{crossover}|G_c(j\omega_{gain\ crossover})|R_2} \quad (22)$$

$$R_1 = \frac{R_2}{K_{value}-1} \quad (23)$$

$$C_3 = C_2(K_{value} - 1) \quad (24)$$

$$\omega_{pk} = \omega_{gain\ crossover} \cdot K_{value} \quad (25)$$

$$R_3 = \frac{\sqrt{K_{value}}}{\omega_{crossover}C_3} \quad (26)$$

The design of the type III compensator circuit is based on achieving a phase that can approaches -180^0 when the magnitude reaches 0 dB [17]. The use of the K-Factor method determines the locations of poles and zeros based on phase characteristics observed in the

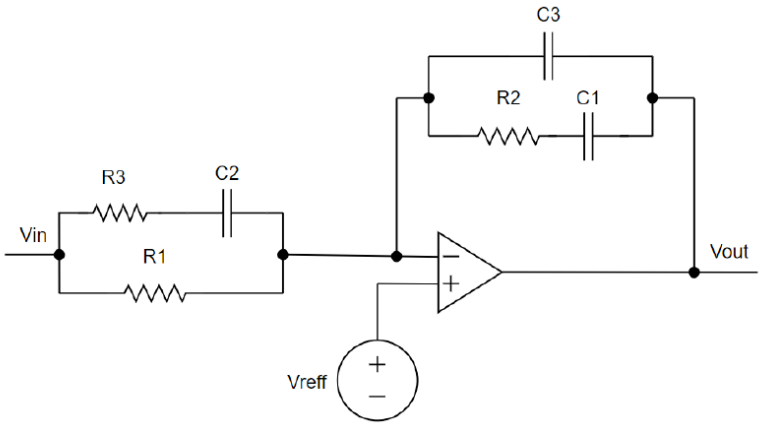

Figure 2. The circuit of the Type III compensator.

Bode plot. The PM values to be simulated using MATLAB software are 60°. A 60° PM was chosen as the design target because it provides a widely accepted balance between fast transient response and robust stability [20].

Figure 3 presents the Bode plot obtained from MATLAB based on a 60° PM design target. The magnitude plot crosses 0 dB at approximately 6.2×10^4rad/s (~10 kHz). The corresponding phase at this frequency is approximately −120°, indicating that the loop satisfies the 60° PM specification. Note that the goal is not to force the phase to reach −180° at crossover, but rather to ensure the sum of the plant and compensator phases remains at least 60° above −180°, guaranteeing stable closed-loop operation. The relationship between PM and overshoot follows standard control theory: larger PM improves damping, resulting in smaller overshoot but slower settling, whereas lower PM increases responsiveness but risks oscillatory behavior.

C. Hardware design

The hardware of the proposed system consists of two main parts: the buck-converter power stage and the supporting control circuitry. To enable closed-loop regulation, several control-related blocks are implemented: (1) a Type III compensator constructed using an analog RC network for pole–zero shaping; (2) a comparator used to generate the error signal between the reference and feedback voltage; (3) a PWM generator implemented on the microcontroller operating at 146 kHz; and (4) a gate-driver stage that provides the required current to drive the MOSFET gate. Together, these blocks form the complete closed-loop control system as shown in Figure 4.

D. Performance testing method

All performance testing in this study was carried out on the hardware prototype using a digital oscilloscope (GW INSTEK GDS-1052-U). For each experiment, the

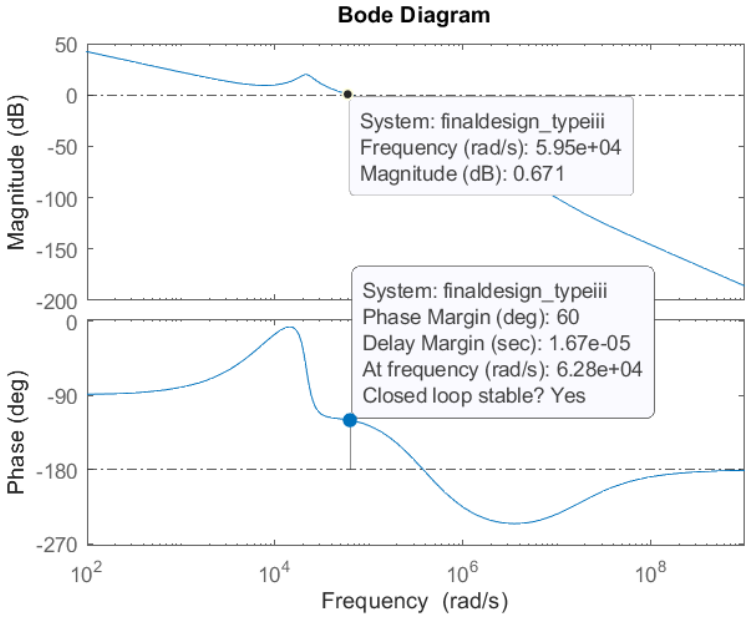

Figure 3. Frequency response analysis for 60° PM.

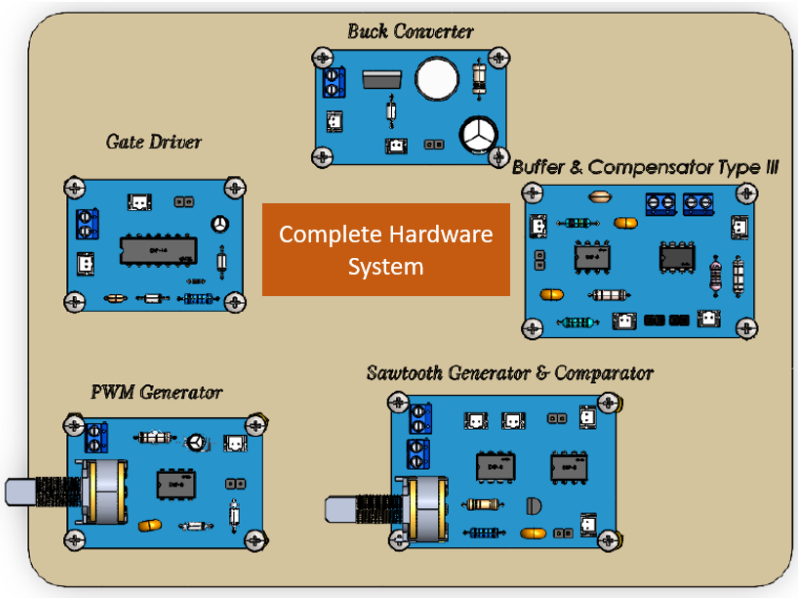

Figure 4. Hardware design of the proposed buck-converter.

converter was powered from 0 V so that the full startup transient could be captured. Two load categories were evaluated: resistive loads in various series/parallel configurations, and DC-motor loads with different electrical characteristics. During each test, the output voltage waveform was recorded, and the following key performance metrics were extracted: overshoot, undershoot, settling time, and steady-state voltage. The steady-state voltage was included to quantify steady-state regulation and to infer steady-state error relative to the 6-V target output.

These parameters were selected because they directly represent the dynamic and steady-state behaviours most relevant to buck-converter applications implemented on low-cost microcontrollers. Rise time and peak time were not included in the tables because the oscilloscope measurements prioritized capturing peak deviations and stabilization characteristics which were the main indicators used to evaluate the effectiveness of the type III compensator.

III. Results and Discussions

In this work, simulation, and hardware were used for different purposes. The LTspice simulation was employed only for the design of the type III compensator, where the small-signal model was analyzed to verify the desired PM and place the poles and zeros appropriately. The compensator parameters obtained from the simulation were then implemented directly in the hardware prototype. All performance evaluation, including transient response, overshoot, undershoot, settling time, and steady-state regulation, was carried out entirely on the hardware system. Two types of loads were tested in the experiment: resistive loads and DC-motor loads. The hardware test results, therefore, represent the real dynamic behavior of the converter under practical operating conditions, whereas the simulation served as a preliminary design tool rather than a performance-testing platform.

A. Resistive load

The transient-response results for the open-loop and closed-loop systems are summarized in Table 1 and Table 2. In the open-loop configuration, the buck converter exhibits modest overshoot in cases where the peak voltage exceeds the final steady-state value, for example, the 300 Ω load produces a peak of 4.4 V against a 4.2 V steady-state level. However, the settling times are consistently long, ranging from 85 ms to 114 ms, indicating a slow dynamic response. The steady-state voltage varies widely from 4.2 V to 6.6 V across the tested loads, reflecting poor regulation and sensitivity to load changes. The undershoot observed during transients ranges from 1.0 V to 3.0 V which corresponds to drops of approximately 17 % to 76 % below the respective steady-state values. These deep voltage dips highlight the open-loop system's vulnerability to sudden load transitions and its inability to maintain stable output regulation.

When the same tests were conducted using the type III compensator, the overall dynamic performance improves substantially. Overshoot is eliminated for nearly all resistive loads, except for the 300 Ω//10 kΩ case, which shows a small overshoot of 6.2 V relative to the 6.0 V steady-state value (approximately 3.3 %). The most significant improvement is observed in the

Table 1.
Resistive load: open loop.

No	Load	Overshoot (V)	Undershoot (V)	Steady state (V)	Settling time (ms)
1	300 Ω	4.4	1.0	4.2	113
2	1 KΩ	-	1.4	4.6	107
3	10 KΩ	5.0	2.6	6.4	85
4	300 Ω + 1 KΩ	5.2	3.0	6.6	89
5	300 Ω // 1 KΩ	-	1.6	4.6	110
6	300 Ω + 10 KΩ	-	2.8	6.6	110
7	300 Ω // 10 KΩ	-	1.0	4.2	114

Table 2.
Resistive load: type III compensator.

No	Load	Overshoot (V)	Undershoot (V)	Steady state (V)	Settling time (ms)
1	300 Ω	-	5.0	6.0	4.2
2	1 KΩ	-	5.0	6.0	4.6
3	10 KΩ	-	5.6	6.0	0.39
4	300 Ω + 1 KΩ	-	5.4	6.0	3.9
5	300 Ω // 1 KΩ	-	5.0	6.0	3.8
6	300 Ω + 10 KΩ	-	5.6	6.0	0.51
7	300 Ω // 10 KΩ	6.2	5.0	6.0	3.8

settling time, which is reduced to 0.39–4.6 ms, representing a performance gain of roughly 95 %–99.5 % compared to the open-loop configuration. The steady-state voltage was consistently regulated at 6.0 V across all loads, demonstrating the compensator's ability to enforce accurate voltage control. The undershoot values listed in Table 2 (5.0–5.6 V) correspond to actual voltage dips of only 0.4–1.0 V, or approximately 6.7 %–17 % below the 6-V steady-state level. These dips are significantly smaller than those in the open-loop case, confirming that the type III compensator not only accelerates transient recovery but also substantially reduces the severity of voltage dips during disturbances.

In the hardware testing, the transient waveform was captured using a digital oscilloscope to observe the system's dynamic response. Figure 5 shows the output voltage under a 300 Ω resistive load. At startup, the voltage rises to approximately 5.8 V, followed by a brief dip to 5 V lasting about 4.2 ms. The output then increases smoothly until it reaches the steady-state value of 6 V. This behavior confirms that the closed-loop type III compensated system is capable of regulating the output voltage with minimal deviation and achieving stable operation.

A comparison with the findings in reference [17] provides additional context for the observed performance. reference [17] demonstrates a digitally

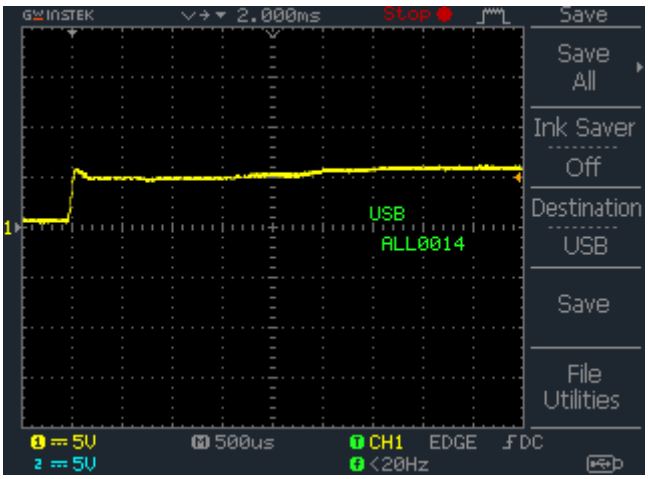

Figure 5. Transient response for 300 Ω resistor load with type III compensator.

implemented type III compensator with optimized pole–zero placement, achieving extremely fast transient performance due to high crossover-frequency operation. However, its evaluation is limited to modeling and simulation rather than hardware testing. In contrast, the present study implements the compensator on a low-cost microcontroller and validates its behavior experimentally under practical resistive loads. Although the transient performance achieved here is slower than the theoretical results reported in [17], the proposed implementation delivers stable regulation and consistent steady-state behavior using simple tuning and inexpensive components. This demonstrates the trade-off between theoretical optimality and practical realizability, highlighting the suitability of the proposed design for low-cost, educational, and prototype-level applications.

B. DC-motor load

The second evaluation was conducted using three types of DC motors, each exhibiting inductive characteristics and high inrush current during startup. Table 3 summarizes the open-loop results. Because the system does not reach the 6-V target, no overshoot is observed. The steady-state voltage settles only at 4.0–4.2 V (67–70 % of nominal), indicating a large steady-state error. The undershoot values of 3.0–3.6 V correspond to dips of 0.4–1.2 V (7–20 %) relative to the steady-state level. Settling times are long, 116–134 ms, confirming that the open-loop configuration exhibits slow dynamic recovery and inadequate voltage regulation for motor loads.

When the same motors were tested with the type III compensator (Table 4), the dynamic behavior changed dramatically. Overshoot increases to 8.4–9.2 V, equivalent to 140–153 % of the 6-V nominal output. This large overshoot is expected, as the compensator responds aggressively to counteract the motor's startup current surge and back-EMF. Despite the higher overshoot, the settling time improves by approximately 97–99 %, decreasing from 116–134 ms in the open-loop system to only 1.5–5.2 ms. Steady-state voltage regulation also improves substantially, reaching 5.0–6.0 V (83–100 % of nominal). The undershoot values (3.4–5.0 V) should be interpreted relative to the improved steady-state voltage. For instance, a dip from 6.0 V to 5.0 V represents a 1.0 V (17 %) drop, smaller than the 1.2 V (20 %) dip observed in the open-loop system. Although the absolute voltage values appear higher, the actual deviation from steady state is smaller due to the improved nominal operating point.

A comparison between the two configurations highlights the trade-off clearly. The open-loop system produces lower peak voltages but suffers from slow settling and large steady-state errors, making it unsuitable for supplying inductive motor loads. In contrast, the type III compensator provides rapid stabilization and significantly improved voltage regulation at the expense of higher overshoot, an expected compromise when pursuing higher loop bandwidth and faster response.

Figure 6 shows the transient response of the converter when supplying a type-130 DC motor. At startup, the output voltage momentarily rises to 8.4 V, then dips to approximately 5 V before undergoing small oscillations and settling at 6 V within about 1.3 ms. The large initial overshoot occurs because the motor's current surge briefly pulls the output downward, prompting the compensator to increase the duty cycle aggressively. Once the transient subsides, the control loop stabilizes and maintains the desired output. This waveform illustrates both the fast-settling capability and the assertive corrective action characteristic of the implemented type III compensator when driving inductive motor loads.

Table 3.
DC motor load: open-loop.

No	DC-motor type	Overshoot (V)	Undershoot (V)	Steady state (V)	Settling time (ms)
1	130	-	3.0	4.0	133
2	N30	-	3.6	4.2	116
3	RF-300	-	3.2	4.0	134

Table 4.
DC motor load: type-III compensator.

No	DC-motor type	Overshoot (V)	Undershoot (V)	Steady state (V)	Settling time (ms)
1	130	8.4	5.0	6.0	1.5
2	N30	9.2	4.2	5.6	3.9
3	RF-300	9.2	3.4	5.0	5.2

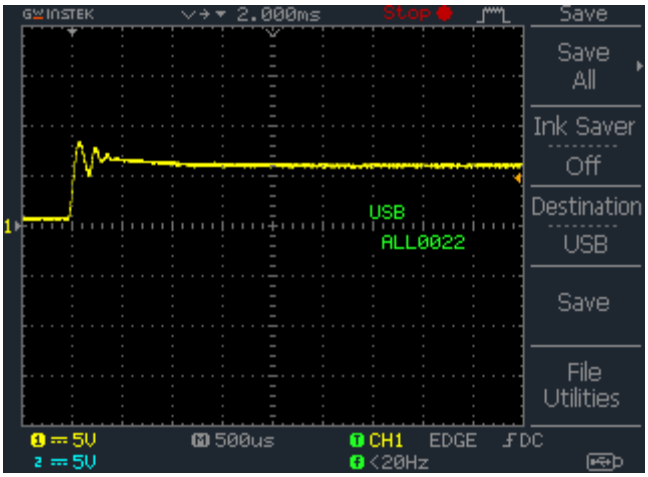

Figure 6. Transient response for DC-motor type 130 load with type III compensator.

IV. Conclusion

The implementation of the type III compensator in the buck converter yields a measured PM of approximately 60°, selected to provide a practical balance between stability robustness and transient response. Experimental results confirm that the compensator significantly improves dynamic performance under resistive loads: settling time decreases from tens of milliseconds in the open-loop system to below 5 ms in the closed-loop configuration, an improvement of one to two orders of magnitude depending on the load. The steady-state output is also more tightly regulated, with substantially smaller voltage dips during transient disturbances. However, overshoot increases as a result of the higher loop bandwidth and the more assertive corrective action required for fast stabilization, representing an inherent trade-off when prioritizing transient speed. For DC-motor (inductive) loads, the compensator shows limited ability to suppress overshoot and maintain the target steady-state voltage. This limitation arises because the controller was designed using a small-signal model that assumes purely resistive loading and therefore does not capture inductive-load characteristics such as back-EMF, high startup currents, and mechanical inertia. As a result, the controller performs well for resistive conditions but becomes less effective for loads with strong dynamic behavior. Future work should incorporate load-dependent modeling and compensator retuning to enhance performance across a wider range of practical operating conditions.

Declarations

Author contribution

All authors contributed equally as the main contributor of this paper. All authors read and approved the final paper.

Funding statement

This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

Competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The use of AI or AI-assisted technologies

During the preparation of this study, the author(s) used ChatGPT to improve readability and language. After using this tool/service, the author(s) reviewed and edited the content as needed and took (s) full responsibility for the content of the publication.

Additional information

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