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Design and Implementation of Capacitor Array as DC Converters for Electrical Lighting in limited Area

Arman Jaya ^{a,*}, Irianto ^b, Afif Aulia Rahman ^c, Kyungmin Sung ^d

Abstract

The widely used DC-DC converters are inductor-based DC-DC converters and inductors along with combustion. The use of inductors can lead to large power losses, as well as heavy components in real terms. The proposed converter warning array aims to increase the voltage with a large increase ratio through a switching configuration process. This switching method is very simple and uses two pulses that are opposite each other so that the array converter can work optimally, whose function is to adjust the arrangement in a parallel arrangement to a series arrangement. The advantage of using a device is that it makes DC-based DC conversion lightweight and easy to implement. Tests have been carried out on 5 hanger arrays with a power of 80 W and 65 W, and the data from the test results show that the voltage increase ratio reaches 81.5% or 4.08 times the input voltage, which indicates that the array converter warning is able to increase the input voltage according to the number of the arrays.

Keywords: Inductor-based converter, Inductor and capacitor-based converter, Capacitor Array

I. INTRODUCTION

At this time, the use of dc converters to increase and or decrease the input voltage is widely used in several applications such as dc houses, battery charging, and so on. DC converters that have been widely implemented are dc converters that use inductors[1],[2]. This type of converter can increase and decrease the input voltage by using a variable duty cycle ratio [3] as well as using the transformer winding ratio for a significant increase in voltage levels. In addition, during switching transitions, it can cause transformer leakage at high frequencies[4][5], as well as requiring an air gap to prevent core saturation due to high DC currents[6],[7].

To raise the ratio level to a high level also developed a converter that combines the functions of the inductor and capacitor[8],[9], as also represented by[10],[11] the structure uses two inductors assisted by a transformer ratio for the input voltage step of 45 V to 450 V output from the capacitor. In [12],[13] it was also introduced the use of 2 inductors and a pump capacitor at the input to store and distribute energy to the load.

However, in addition to this complicated converter and the presence of power losses due to switching, it can reduce the performance of this converter[14].

A switching capacitor converter has been introduced in [15], which focuses on the characteristics of the switching process. In [16],[17] a switching capacitor converter that analyzes the power loss during the switching transition is also introduced. The switching capacitor converter that was introduced before has not analyzed the increase in the resulting input voltage over a larger range, some at zero voltage switching [18]. The topology introduced focuses on analyzing the increase in input voltage based on the arrangement of capacitors using the capacitor switching method. In addition to the components used is quite simple, using only MOSFETs and capacitors, systems that are lightweight and also have high efficiency, as well as smaller switching losses[19][20], the topology introduced a [7] has a different structure, where the capacitor is charged in a parallel configuration, and discharged in a series configuration, to

generate an output voltage equal to the input voltage multiplied by the number of capacitor arrangements.

II. METHODOLOGY

The input voltage level is increased by a capacitor array using 2 switching configurations that function to change the arrangement of the

capacitor. Capacitor charging is regulated through a number of switches for parallel configuration, while the increase in voltage level occurs when the capacitor is in series.

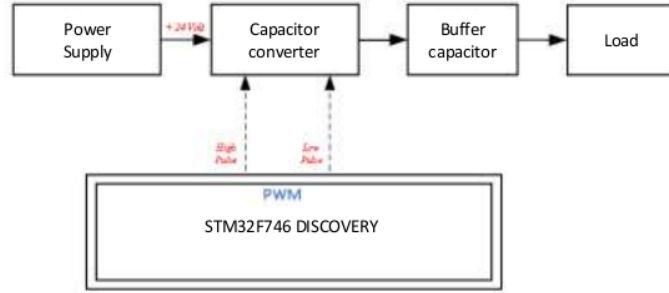


Figure 1. Block diagram of the capacitor array system

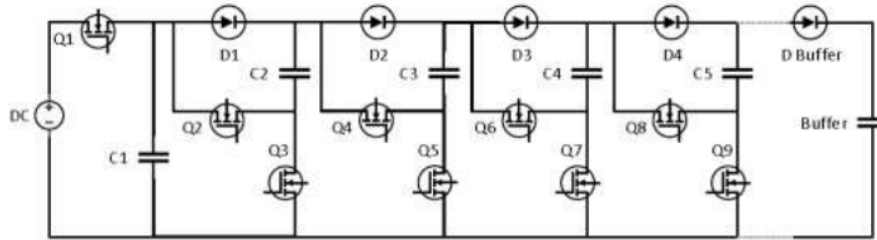


Figure 2. Array capacitor topology

Figure 1 shows the use of microcontrollers. In this system, namely to generate PWM opposite each other visited on MOSFET drivers with specifications that are able to accept switching with high frequencies, so that the switching configuration on the capacitor converter array can work optimally.

The proposed capacitor array, as shown in Figure 2, has 5 total capacitor arrangements with 1 buffer capacitor. The capacitor array charges when switches Q1, Q3, Q5, Q7, Q9 is on and switches Q2, Q4, Q6, Q8 is off. D1, D2, D3, and D4 are forward biased, so that the capacitor in parallel arrangement with the amount of charging voltage can be calculated by the following equation:

$$V_C(t) = V_s(t)(1 - e^{-\frac{t}{RC}}) \quad (1)$$

where :

$V_C(t)$ = Charging voltage across the capacitor (V)

$V_s(t)$ = Input voltage (V)

RC = Time constant (s)

t = charging time in capacitor(s)

e = Euler's number is 2.7182

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_{C5} = 0.99V_{in} \quad (2)$$

where :

$V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_{C5}$ Voltage across capacitors 1 to 5 (V)

To raise the input voltage level, the capacitor releases its charge to the load when the switches Q2, Q4, Q6, and Q8 are on and switches Q1, Q3, Q5, Q7, and Q9 are off. D1, D2, D3, and D4 reverse biased, so that the capacitors are in series. The amount of voltage received by the buffer capacitor is the sum of the discharge voltages on each capacitor.

$$V_o(t) = V_C(t) \times e^{-\frac{t}{RC}} \quad (3)$$

where :

$V_o(t)$ = Output voltage capacitor (V)

$V_C(t)$ = The voltage is stored in the capacitor (V)

RC = Time constant (s)

t = charging time in capacitor (s)

e = Euler's number 2.7182

Figures 3a and b show the operating principle of the capacitor array.

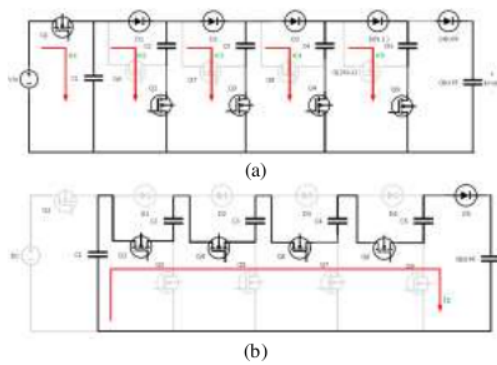


Figure 3. (a) Array Capacitor Charging,
(b) Array Capacitor Discharging

The capacitor array has 5 total capacitors with two circuit configurations as shown in Figure 3. In charging mode, the 12 capacitors are in a parallel configuration, and the voltage across capacitor 1 is equal to capacitor 2 to 5. In ideal conditions, the charging voltage across the capacitor is equal to the input voltage, which is 24 Vdc. This is in accordance with the nature of the capacitor, which is that it can store voltage according to the input given. In discharging mode, the capacitors are in a series configuration. The 21 voltage stored on each capacitor accumulates and the output voltage is 5 times the input voltage, according to the series configuration in Figure 3.

The buffer capacitor value of the capacitor array must be able to accommodate the total voltage resulting from the sum of the voltage multiplier capacitors, so as to design the buffer capacitor value using the highest power of the load to be used. The amount of the buffer capacitor can be calculated by the following equation :

$$C_{buff} \gg \frac{P_o}{\frac{1}{2}V_o^2} \quad (4)$$

where :

C_{buff} = Buffer capacitor (μ F)

P_o = Capacitor output power (W)

$V_o(t)$ = Capacitor output voltage (V)

III. RESULT AND DISCUSSION

The proposed system is built using component specifications as shown in Table 1.

Table 1.
Array capacitor parameters

Parameter	Unit
DC Input voltage	24 V
DC output voltage	110 V
Switching frekuensi minimum	5 kHz

Capacitor	22 μ F
Capacitor Buffer	10k μ F
Diode	MUR1560 (Fast Recovery)
Switch Q	MOSFET IRF460

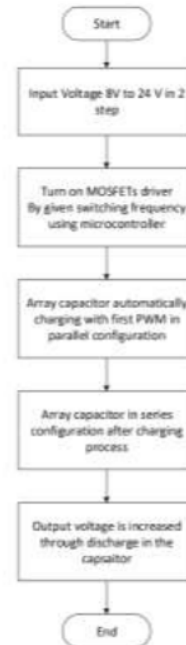


Figure 4. Flowchart experiment array capacitor

Figure 4 is a summary of the work system of the capacitor array, which has 5 process stages. From this process, the importance of the MOSFET driver so that the capacitor array can optimally work in parallel and series configurations. The parameters above are the parameters used in the converter capacitor array system with the component specifications that have been taken into account. The most important part of this system is maximizing the performance of the switching generated by the microcontroller via the MOSFET driver. The use of IRFP460 MOSFET type is able to handle high switching frequencies up to 1 Mhz, so it is safe during prototype testing.

The testing process uses a power supply as the input voltage and a load of 3 lamps arranged in parallel, which are turned on alternately to regulate the amount of load power that must be supplied by the capacitor array. The experiment uses 2 voltmeters installed at the input and output the capacitor array to determine the actual increase in the input voltage ratio. The magnitude of the switching frequency is controlled using a microcontroller, according to Table 2.

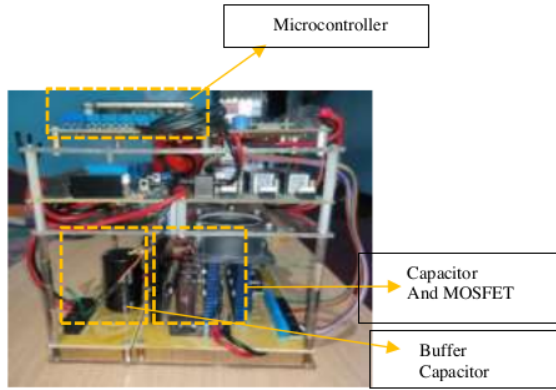


Figure 5. Array capacitor prototype

Figure 5 represents the hardware designed to the specifications in Table 1, with a minimum planned switching frequency of 5 kHz, which is passed on to the MOSFET driver. The MUR 1560 fast recovery diode functions as a controlless switch when the capacitor is in a parallel configuration. The capacitor used is 22 μ F with a voltage capacity of 400 V, in order to be able to receive input voltage when the charging process is in a high frequency of 20 kHz.

Table 2.
Data from testing the capacitor array for 80 W and 65 W power

f (kHz)	V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)	$\frac{V_o}{V_{in}}$	P_{out} (W)	Load
5	8	2.51	21.4	0.43	2.6	9.21	80 W
	12	3.28	38.6	0.54	3.2	20.8	
	16	3.4	56.6	0.64	3.5	36.2	
	20	4.5	74.7	0.74	3.7	55.3	
	24	5.17	96	0.84	3.9	79.9	
10	8	2.82	21.9	0.43	2.7	9.43	
	12	3.71	39	0.54	3.24	21.0	
	16	4.5	57	0.65	3.55	37.1	
	20	5.16	75.4	0.74	3.75	55.7	
	24	5.78	97	0.83	3.91	80.8	
20	8	7.39	20.4	0.37	2.52	8.58	
	12	11	36.7	0.47	3.05	19.4	
	16	14.87	54.5	0.58	3.4	34.3	
	20	18.72	72.7	0.68	3.62	53.0	
	24	23.08	93.5	0.77	3.8	77.6	
5	8	1.87	24.1	0.309	2.97	7.45	65 W
	12	2.55	41.5	0.40	3.45	16.8	
	16	3.15	59.3	0.496	3.69	29.4	
	20	3.64	78.2	0.57	3.89	44.6	
	24	4.15	99.8	0.65	4.05	64.7	
10	8	2.28	24.3	0.31	2.99	7.48	
	12	3.12	41.9	0.41	3.47	16.7	
	16	3.86	59.8	0.49	3.71	29.3	
	20	4.44	78.6	0.57	3.89	44.6	
	24	4.97	100	0.65	4.07	65.2	
20	8	3.2	22.3	0.29	2.75	6.43	
	12	4.56	38.5	0.39	3.2	15	
	16	5.63	56.4	0.43	3.51	27.0	
	20	6.45	74.2	0.56	3.69	41.5	

	24	7.12	96	0.64	3.91	61.8	
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Table 2 shows the data from the test results of the array capacitor at a load of 80 W and 65 W. Input voltage is increased in 2 Volt steps from 8V to 24V at each switching frequency of 5 kHz to 20 kHz. For a power of 80 W at a nominal input voltage of 24 V, resulting output voltage reaches 3.8 times the input voltage. There is a difference in the power of 65 W at a nominal input voltage of 24V, reaching multiples of 4.07 times. The switching frequency affects the amount of charging current in the capacitor when the parallel configuration is configured. The magnitude of the switching frequency is proportional to the magnitude of the charging current in the capacitor because the capacitor is forced to charge in a faster time which causes heat in the capacitor. This can be seen at a power of 80 W. A switching frequency of 20 kHz reduces the ratio of the increase in input voltage, due to the inability of the capacitor to receive a charging current that is too large. Figure 6 is an image of the testing process of the capacitor array at a switching frequency of 20 kHz and a load of 80 W. This test uses a power supply with a capacity of 450 W with input voltage steps, as

shown in Table 2. In addition, the capacitor array has also been simulated using PSIM software to compare the simulation results with direct hardware testing with the same capacity and specifications. The following is a comparison of the simulation results.

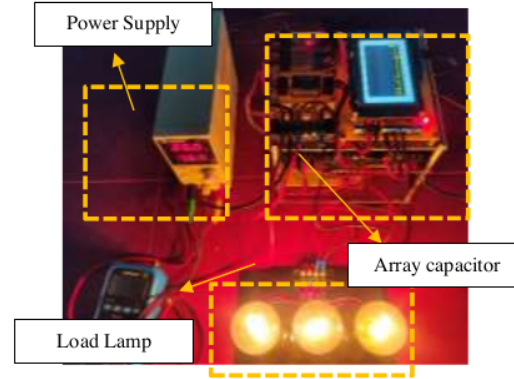
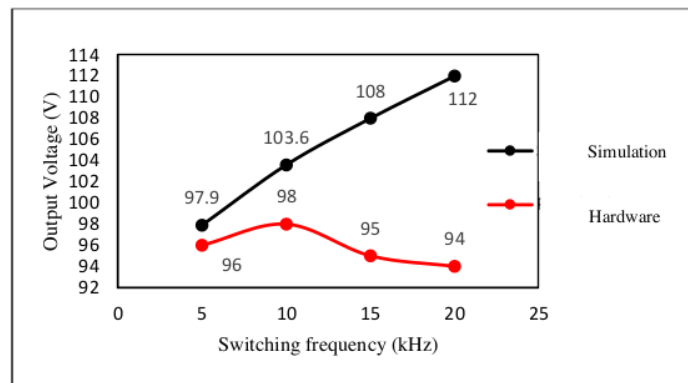
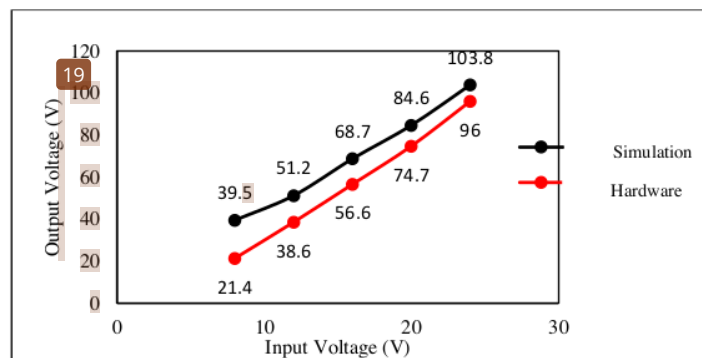


Figure 6. Array capacitor test



(a)



(b)

Figure 7. (a) Comparison of simulation and hardware on changes in switching frequency

(b) Comparison of the ratio of the simulated output voltage level and the hardware at a change in input voltage f 10 kHz

Figure 7 shows the experimental results at a maximum power of 100 W. Minimum switching frequency given is 5 kHz and varied up to 20 kHz can be seen in the simulation comparison results. At minimum frequency, the simulation voltage ratio reaches 81.58%, while the hardware test results reach 80%. The maximum increase level achieved on hardware is 10 kHz with an increased ratio of 81.05%, while the simulation is higher, namely 86.3%. There is a saturation of the capacitor at a frequency of 15 kHz, which causes a decrease in the increase in the voltage ratio of 79.1%. This is due to the inability of the capacitor to accept large charging currents at a frequency of 15 kHz. So that when the frequency is increased to 20 kHz, the reduction ratio is even greater, reaching 77%. The effect of an extensive charging current can increase the temperature of the capacitor if, for a long time, it can reduce the resistance of the capacitor. In the test conditions above, the maximum frequency that the capacitor can receive to work optimally is 15 kHz. This means that to increase the input voltage from the power supply, the optimal frequency must be given 15 kHz.

The comparative results of hardware testing and simulation have shown that the converter capacitor array has succeeded in increasing the input voltage up to 4 times by using the switching method. It can be seen that the comparison of the percentage increase between the simulation and the hardware is quite small at each switching frequency. At a frequency of 10 kHz, as shown in Table 2, it is known that the capacitor array is capable of supplying power according to the design, namely a maximum of 80 W, with a generated power of 80.8 W. generated by the capacitor array of 65.2 W. While the comparison of the results of the ratio of the increase in the output voltage of the simulation and hardware as shown in Figure 7, that the simulation has a greater increase ratio of 5% compared to the hardware test results because the components used in the simulation are in ideal conditions so that there is no diode voltage drop even in the switching process, whereas, at the knee voltage hardware on the diode, the presence of a large switching frequency becomes a factor in reducing the increase in output voltage ratio.

IV. CONCLUSION

The results of the capacitor array have been discussed in section 3, which shows that the capacitor array is able to increase the voltage up to 4 times the input voltage of 24 Vdc, with a

percentage of 81.05% in hardware and 86.3% in the simulation, which shows that the switching capacitor method successfully configures the array of the capacitor to increase the voltage. In addition, the capacitor array is capable of supplying 80W of power with an output voltage of 98 Vdc with an increase in voltage level ratio of 3.9 times the input voltage. At 65 W, the output voltage of the capacitor array reaches 100 Vdc and the gain ratio is 4 times that of the input voltage.

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